

MILLIMETER-WAVE INTEGRATED CIRCUIT DESIGN IN SILICON-GERMANIUM TECHNOLOGY FOR NEXT GENERATION RADARS

A Thesis
Presented to
The Academic Faculty

by

Peter Song

In Partial Fulfillment
of the Requirements for the Degree
Master of Science in
Electrical and Computer Engineering



School of Electrical and Computer Engineering
Georgia Institute of Technology
May 2014

Copyright © 2014 by Peter Song

MILLIMETER-WAVE INTEGRATED CIRCUIT DESIGN IN SILICON-GERMANIUM TECHNOLOGY FOR NEXT GENERATION RADARS

Approved by:

Professor John D. Cressler, Advisor
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor John Papapolymerou
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Professor Hua Wang
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Date Approved: 7 April 2014

ACKNOWLEDGEMENTS

This thesis would not have been possible without the support of the following people and organizations:

- Dr. John Cressler and Dr. Gregory Sadowy for their wise guidance and invaluable mentorship.
- My committee members, Dr. John Papapolymerou and Dr. Hua Wang for their support.
- The SiGe Devices and Circuits team for keeping the lab a fun place to work – sometimes even during tapeouts.
- NASA’s Office of the Chief Technologist for a wonderful opportunity and support through the NASA Space Technology Research Fellowship.
- IBM Microelectronics and Semtech for access to and assistance with the IBM 9HP SiGe BiCMOS platform.
- Dr. Robert E. Leoni, III, Dr. Nicholas Koliass, and Jeffrey Kotce for their gracious assistance with W-band measurements.
- My friends for their encouragement and for reminding me that there is life outside of tapeout.
- My mother for her unwavering support and love.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS	iii
LIST OF TABLES	vi
LIST OF FIGURES	vii
SUMMARY	ix
1 INTRODUCTION	1
1.1 Motivation	1
1.2 Technology Overview	3
1.3 Design Challenges	5
1.3.1 Device Interconnects	5
1.3.2 Ground Plane	6
1.3.3 Transmission Lines	7
1.3.4 Signal pads	8
2 PHASED ARRAY RADARS	10
2.1 Introduction	10
2.2 Passive Electronically Scanned Array	11
2.3 Active Electronically Scanned Array	12
2.4 Transmit-Receive Module	14
3 W-BAND SINGLE-POLE DOUBLE-THROW SWITCH	17
3.1 Introduction	17
3.1.1 Single-pole Single-throw	17
3.1.2 Single-pole Double-throw	18
3.2 Design of a W-band Single-pole Double-throw Switch	19
3.2.1 p-i-n Diodes	19
3.2.2 SPDT Topology	19
3.2.3 Generalized Design Procedure	23
3.3 Measurement Results	24

3.4	Performance Comparison	28
4	W-BAND LOW-NOISE AMPLIFIER	31
4.1	Introduction	31
4.1.1	Noise in Cascaded Systems	31
4.1.2	Noise Figure Measurement	32
4.2	Design of a W-band Low-noise Amplifier	33
4.2.1	Generalized Design Procedure	33
4.2.2	LNA Topology	35
4.2.3	Matching Networks	36
4.3	Measured Results	39
4.4	Performance Comparison	43
5	CONCLUSION	45
5.1	Future Work	45
	REFERENCES	47

LIST OF TABLES

1	Comparison of State-of-the-Art W-band SPDT Switches	30
2	Comparison of State-of-the-Art W-band SPDT LNAs	44

LIST OF FIGURES

1	An artist's rendition of the CloudSat satellite [15]	2
2	Simplified cross-sectional diagram of a SiGe HBT in IBM 8HP	4
3	Cross-sectional diagram of back-end-of-line metallization of IBM 9HP	5
4	Sonnet 3D view of metal interconnects for a CBEBC HBT	6
5	Sonnet 3D view of a GSG pad	9
6	Sonnet electromagnetic simulation setups of a GSG pad	9
7	The US Army's SCR-270 radar setup in Pearl Harbor, HI [6]	11
8	Examples of PESA radars	12
9	TI's MERA transmitter, multiplier, and receiver module [9]	13
10	PAVE PAWS at Clear Air Force Station, Alaska [31]	13
11	Block diagram of a typical transmit-receive module with shared common-leg circuitry	15
12	Block diagrams of SPST and SPDT switch configurations	18
13	Cross-sectional diagram of a vertical p-i-n diode in a SiGe BiCMOS technology	19
14	Series p-i-n diode on- and off-state S-parameters over anode area at 94 GHz and V_{ac} of 1 V	20
15	Shunt p-i-n diode on- and off-state S-parameters over anode area at 94 GHz and V_{ac} of 1 V	21
16	On- and off-state shunt resistance and off-state shunt capacitance over p-i-n diode anode area at 94 GHz	22
17	p-i-n diode equivalent models including via parasitics	23
18	Schematic and chip micrograph of the W-band SPDT switch	25
19	Measured versus simulated S-parameters of SPDT switch in the thru state	26
20	Measured versus simulated s-parameters of SPDT switch in the isolation state	26
21	Measurement setup for large-signal characterization at W-band	27
22	IV characteristic of the thru path of the SPDT showing the large-signal voltage swing headroom for a V_{SW} of -4 V	28

23	Measured output power and gain across input power of the SPDT switch at 92 GHz	29
24	NF_{min} and G_{max} for a common-emitter CBEBC HBT with inductive emitter degeneration at 1.2 V_{CE} and 0.65 mA/ μ m I_C from 75–110 GHz vs emitter length, L_E , in IBM 9HP	35
25	Γ_{in} and Γ_{opt} for a common-emitter CBEBC HBT with inductive emitter degeneration at 1.2 V_{CE} and 0.65 mA/ μ m I_C from 75–110 GHz vs L_E in IBM 9HP	36
26	Comparison of cascaded common-emitter stages versus a cascode for 4 μ m emitter length devices at 94 GHz at 0.3 V_{CB} and 0.65 mA/ μ m I_C	37
27	Matching network schematic of a single stage of the LNA	38
28	Smith Charts of the matching networks of a single stage of the LNA over 75–110 GHz	38
29	Schematic of the W-band LNA	39
30	Chip micrograph of the W-band LNA	40
31	Measurement setup for W-band noise figure	41
32	Measured versus simulated s-parameters and noise figure	41
33	Measured versus simulated noise figure and associated gain versus V_{cc}	42
34	Measured output power and gain across input power at 94 GHz versus V_{cc}	43

SUMMARY

In this thesis, the circuits which comprise the front-end of a millimeter-wave transmit-receive module are investigated using a state-of-the-art 90 nm SiGe BiCMOS process for use in radar remote sensing applications.

In Chapter I, the motivation for a millimeter-wave radar in the context of space-based remote sensing is discussed. In addition, an overview of Silicon-germanium technology is presented, and the chapter concludes with a discussion of design challenges at millimeter-wave frequencies.

In Chapter II, a brief history of radar technology is presented – the motivations leading to the development of the transmit-receive module for active electronically scanned arrays are discussed, and the critical components which reside in nearly every high-frequency transmit-receive module are introduced.

In Chapter III, the design and results of a W-band single-pole, double-throw switch using SiGe p-i-n diodes are discussed. In particular, the design topology and methods used to achieve low-loss and high power handling over a wide matching bandwidth without sacrificing isolation are described. This work, entitled, "A High-Power, Low-Loss W-band SPDT Switch Using SiGe PIN Diodes," was accepted for presentation at the IEEE Radio Frequency Integrated Circuits Symposium in Tampa, FL, in June, 2014.

In Chapter IV, the design and results of a W-band low-noise amplifier using SiGe HBT's are discussed. The design methodologies used to achieve high gain and exceptional noise performance over a wide matching bandwidth are described. This work, entitled, "A High Gain, W-band SiGe LNA with Sub-4.0 dB Noise Figure,"

was accepted for presentation at the IEEE International Microwave Symposium in Tampa, FL, in June, 2014.

Concluding remarks and a discussion of future work are in Chapter V.

CHAPTER 1

INTRODUCTION

1.1 Motivation

As climate change has become an undeniable part of our daily lives, our ability to predict its effects is becoming increasingly integral to our capacity to form educated and non-reactionary decisions for the weather and climate related issues that we will face in the decades to come. The National Research Council (NRC) Decadal Survey (2003) has estimated that 2-3 trillion dollars of the United States gross domestic product is sensitive to weather and climate events [25]. Since nearly a third of our nation's financial output depends upon unknown factors that are observed to be changing, it behooves us to better understand the implications of human influences on the weather and climate. It is also important to know that we cannot begin to develop a profound understanding of how the climate is changing without improving our climate change models to minimize the uncertainty in their predictions.

Recently, the study of the interactions between aerosols, clouds, and radiation as well as the study of the precipitation and ice content within clouds have become important tools for improving the predictions of our current climate change models. Both the National Aeronautics and Space Administration's (NASA) CloudSat mission and the planned joint Japan Aerospace Exploration Agency's and European Space Agency's EarthCARE mission have demonstrated the feasibility and utility of cloud profiling radars (CPR) at W-band for this purpose [27]. While the EarthCARE radar will improve upon the CloudSat implementation by adding Doppler sensing capability for detecting cloud ascension and descension, both implementations lack any scanning capability at W-band, ultimately hindering the accuracy and usefulness of the



Figure 1: An artist’s rendition of the CloudSat satellite [15]

generated datasets due to the extremely narrow swath of measurement. According to Tanelli et al., a W-band CPR with both Doppler and scanning capability will have the ability to “provide more accurate reconstructions of the atmosphere, necessary to advance our atmospheric models” [27].

Outlined in the NRC Decadal Survey (2007), the Aerosol-Cloud-Ecosystem (ACE) mission aims to reduce uncertainty of climate change prediction through studying the roles of aerosols on cloud formation and their tendency to reflect solar radiation [3]. The Decadal Survey calls for a 94 GHz cross-track scanning cloud radar for “measurement of cloud droplet size, glaciation height, and cloud height” [3]; however, the currently proposed implementations do not meet the specified cross-track scanning requirement at W-band due to the complexity and cost associated with such a design in conventional technology [5, 20]. Therefore, it is apparent that in order to meet not only the ACE mission goals, but for all future CPR’s, an alternative method must be developed to implement the cross-track scanning requirement at 94 GHz in a low-cost platform.

This thesis investigates the design and analysis of some of the fundamental building blocks which comprise the front-end of a transmit-receive module using Silicon-Germanium (SiGe) heterojunction bipolar transistors (HBT), which can be used to realize the cross-track scanning requirement of the ACE mission at 94 GHz.

1.2 Technology Overview

As SiGe technology continues to scale to smaller technology nodes, a plethora of mm-wave applications have emerged which require higher levels of integration than ever before. This application space, formerly dominated by compound semiconductor technology due to performance reasons, is currently being taken over by lower-cost SiGe technology. A well-known and hugely advantageous aspect of SiGe technology is its inherent capability to integrate with CMOS technology with high compatibility to the CMOS back-end-of-line. One of the low cost drivers results from its ability to integrate analog and RF blocks together with digital CMOS blocks on the same die to form compact, mixed-signal system-on-chip designs [4]. But the ability to borrow copiously from the CMOS processing platform is the primary driver for the lower cost of SiGe BiCMOS technology as compared to compound semiconductor technologies.

A cross-sectional diagram of a SiGe HBT from IBM's 8HP SiGe BiCMOS technology is shown in Fig. 2. Compared with the standard Silicon (Si) bipolar junction transistor (BJT), the SiGe HBT includes a SiGe alloy in the base region of the transistor. As Germanium (Ge) has about half of the bandgap of Si, the SiGe alloy also has a reduced bandgap as compared to Si. Why is this beneficial? The smaller effective bandgap across a thin base increases the electron injection from the emitter to the base which results in increased current gain. Furthermore, the speed of the Si BJT is typically limited by the relatively slow velocity of the minority carrier diffusion across the base of the transistor. However, SiGe HBT's employ a Ge doping gradient in the base of the transistors which lowers the bandgap over the grading, and this induces

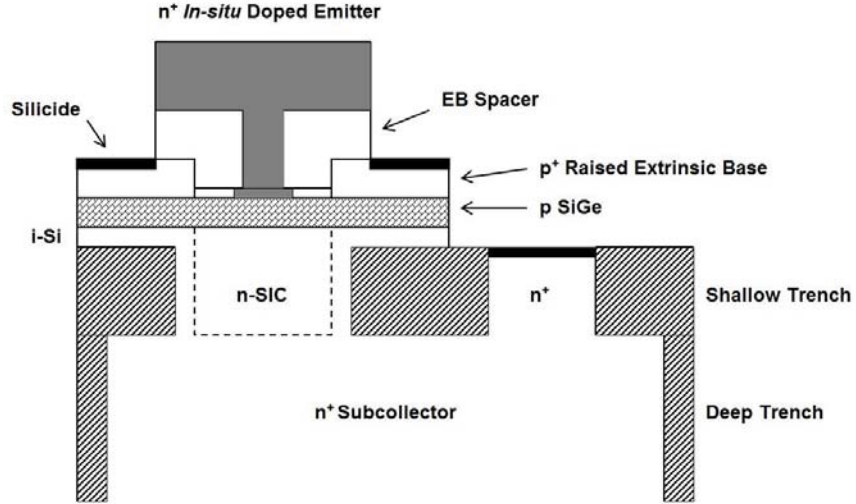


Figure 2: Simplified cross-sectional diagram of a SiGe HBT in IBM 8HP

a drift component to the minority carriers in the base via the created potential field. The drift field lowers the base transit time, thereby reducing a major contribution to the total emitter-collector delay time [4]. The employed “bandgap engineering” in conjunction with selectively-implanted collectors (SIC) brings us to the transistor operation speeds that we observe in modern SiGe HBTs: unity current gain frequency, f_T , up to 350 GHz and unity power gain frequency, f_{max} , up to 500 GHz at the 90-130 nm emitter width technology nodes [8]. Therefore, SiGe HBTs enjoy a 2-3 generation lithographic node performance advantage in comparison to CMOS. As a result, this gives SiGe BiCMOS technologies a cost advantage over CMOS due to the prohibitively high non-recurring engineering (NRE) costs of mask production at highly-scaled CMOS lithographic nodes.

The circuits described in this thesis are fabricated in IBMs 90 nm SiGe BiCMOS technology (IBM 9HP). The process features high-speed SiGe HBTs with $f_T/f_{max}/BV_{CEO}$ of 300 GHz/350 GHz/1.5 V. The 10 metal-layer back-end-of-line (BEOL) consists of four Copper (Cu) digital metals, four Cu intermediate metals, one thick Cu metal,

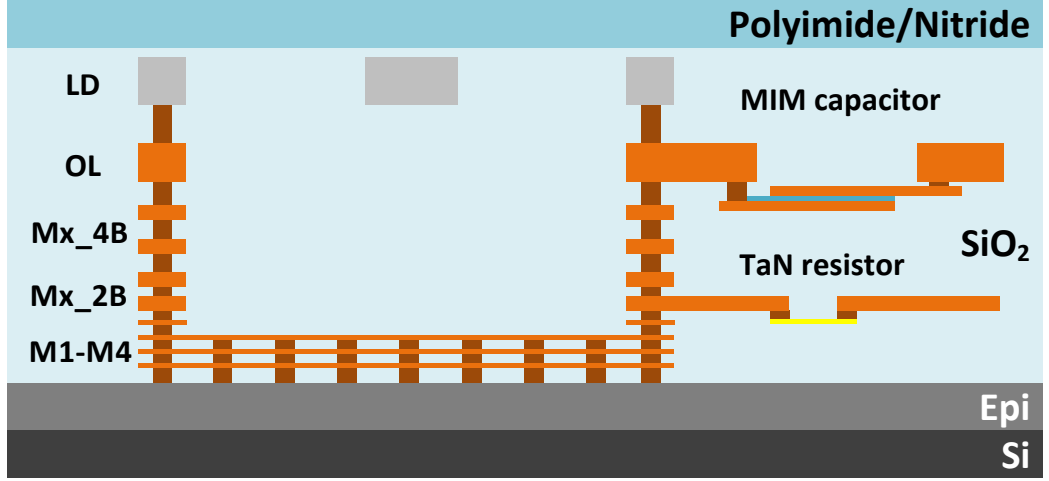


Figure 3: Cross-sectional diagram of back-end-of-line metallization of IBM 9HP

and a thick Aluminum (Al) RF metal, as shown in Fig. 3. The BEOL passive components of interest in this process include high-density metal-insulator-metal (MIM) capacitors and tantalum-nitride (TaN) thin-film resistors.

1.3 Design Challenges

1.3.1 Device Interconnects

At millimeter-wave frequencies the imaginary impedance contribution of device interconnect parasitics is significant. Unconsidered parasitics often make or break a circuit design, and so, the wise millimeter-wave designer will be able to make first order estimates of parasitics for early designs and then verify with electromagnetic simulations for use in final circuit optimization. Therefore, much of the design effort is focused on optimizing layouts to minimize parasitics, eliminating unintended coupling, and modelling to absorb parasitics either into the device models or into the matching networks.

The interconnects leading to the device are modelled from the lowest to the highest metal by fitting equivalent models with series inductance and shunt capacitance on the order of 5-10 pH and 5-10 fF based on electromagnetic simulations, respectively. An example of the device interconnects is shown for an HBT with two collector and

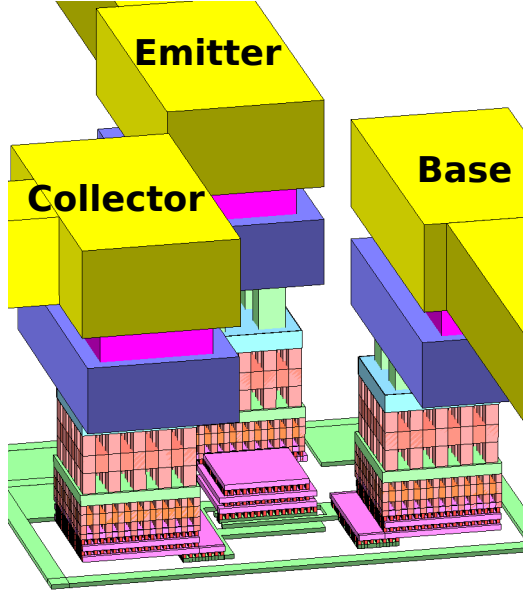


Figure 4: Sonnet 3D view of metal interconnects for a CBEBC HBT

two base stripes (CBEBC) in Fig. 4.

In addition, the millimeter-wave designer will encounter the maximum operating frequency of passives, self-resonant frequency (SRF), due to parasitics, which can spell disaster for circuit designs if not modelled properly.

1.3.2 Ground Plane

The metals used for the device via stack interconnects must meet maximum width and stress design rules while still being wide enough to account for the maximum expected current per unit area, which can cause long-term reliability issues due to electromigration. With the progression to the 90 nm lithography node, the metal fill rules become more strict, especially at the lowest metal levels, in an effort to maintain wafer planarity during BEOL processing.

As a result, the approach taken to form the ground plane is to create a cross-hatch pattern of the lowest level metals where the metal fill rules are the most strict. These metals are connected together using vias generously with an overlapping of metal openings such that the Si substrate is never exposed to transmission lines. A $10 \times$

10 μm^2 unit cell is created and repeated across the entire chip with discontinuities only for devices and bias routing at the lowest metal levels. This method creates an excellent ground plane while effortlessly meeting metal fill and density rules.

1.3.3 Transmission Lines

Unshielded CPW transmission lines cannot be used in Si platforms at millimeter-wave frequencies due to the high dielectric constant, $\epsilon_r = 11.9$, and resistivity, $\rho = 10\text{--}20\ \Omega\text{-cm}$, of the Si substrate without significant losses due to substrate coupling and subsequent re-radiation. In addition, low-loss transmission lines are designed using microstrip lines (MSL's) rather than grounded coplanar waveguide (CPWG) due to the lower loss per unit length achieved using MSL's with the tradeoff of increased potential for line-to-line coupling. Given a typical silicon-dioxide, SiO_2 , dielectric thickness on the order of 8–11 μm , the MSL configuration has significantly lower capacitance per unit length as compared to CPWG. This is because the dominant mode of wave propagation in MSL is quasi-TEM, while the modes of wave propagation in CPWG include both CPW and quasi-TEM, which increases the capacitance per unit length of the CPWG transmission lines. To illustrate some of the implications of transmission line choice, the characteristic impedance, Z_o , of transmission lines obey, to the first order, the simple relationship,

$$Z_o = \sqrt{\frac{L}{C}} \quad (1)$$

Keeping Z_o constant, MSL's require wider signal traces for lower inductance per unit length, which lowers series resistance per unit length as compared to CPWG. Also due to the lower capacitance per unit length, MSL's can obtain higher characteristic impedances than CPWG which allows for the implementation of short transmission lines which act as inductive elements. On the other hand, while CPWG could obtain lower Z_o than MSL with a fixed substrate height, the substrate height can easily be reduced by raising the ground plane to a higher metal level in the stackup.

In IBM 9HP, the MSL's are formed using the thick top-most metal layer, LD, as signal and the bottom-most metals, M1-M4, as ground plane. For a $50\ \Omega$ MSL, $21\ \mu\text{m}$ -wide LD metal is used, and for a $75\ \Omega$ MSL, $5\ \mu\text{m}$ -wide LD metal is used. The $75\ \Omega$ MSL's are useful for matching to certain impedances in a compact matching network even with a slight reduction in Q due to the reduced width of the signal trace.

1.3.4 Signal pads

At millimeter-wave frequencies, the signal pads also need to be considered in matching networks as they present a shunt loading capacitance to the circuit. Using the top metal as signal and the bottom metal as ground in a ground-signal-ground (GSG) configuration, the shunt capacitance of a rectangular signal pad can be estimated using the Palmer capacitance formula to account for the additional fringing capacitance as a first order estimation [19]. The formula for the Palmer capacitance is

$$C_f = \frac{\epsilon WL}{G} \left(1 + \frac{G}{\pi W} \left(1 + \ln \left(\frac{2\pi W}{G} \right) \right) \right) \times \left(1 + \frac{G}{\pi L} \left(1 + \ln \left(\frac{2\pi L}{G} \right) \right) \right), \quad (2)$$

where ϵ is the dielectric constant, W is the width of the signal pad, L is the length of the signal pad, and G is the distance between the signal pad and ground. An example of a GSG pad is shown in Fig. 5.

For a $40 \times 30\ \mu\text{m}^2$ signal pad with $10\ \mu\text{m}$ of SiO_2 between the signal and ground plane with a relative dielectric constant, ϵ_r , of 4.1, the estimated shunt capacitance of the signal pad, C_{pad} , is 8–9 fF. Electromagnetic simulations of signal pads can be performed with two back-to-back simulations, each incorporating one-half of the signal pad as shown in Fig. 6. This method captures both the open half of the signal pad behind the GSG probe and the half of the signal pad which connects to the transmission line leading to the circuit. C_{pad} extracted from the electromagnetic simulations is also 8–9 fF, but in addition, there is 4–6 pH of series inductance that is not accounted

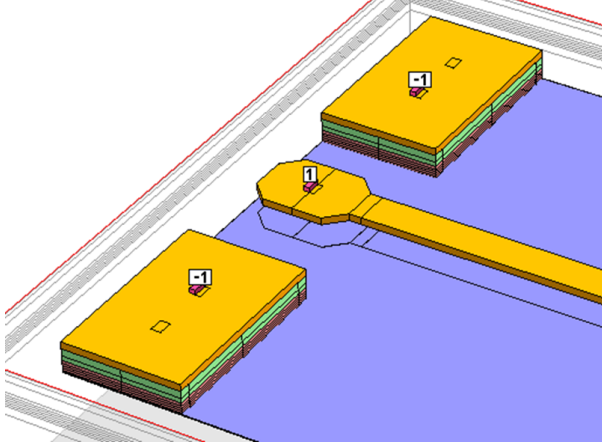


Figure 5: Sonnet 3D view of a GSG pad

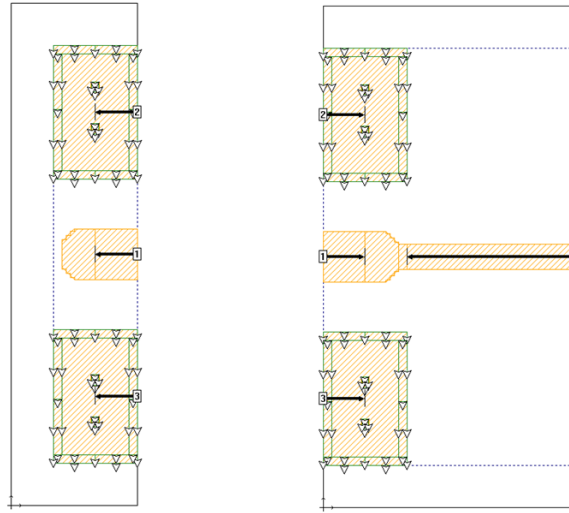


Figure 6: Sonnet electromagnetic simulation setups of a GSG pad

for using the assumed shunt capacitor model approach. Note, that there also exists a parasitic series resistance arising from the contact resistance between the metals of the GSG probe and signal pad, and this will be further discussed in the measured results of the W-band Single-pole Double-throw Switch.

CHAPTER 2

PHASED ARRAY RADARS

2.1 Introduction

The Active Electronically Scanned Array (AESA) is a recent development arising from the intense research and development of semiconductors and radar technology beginning in the 1950's. Some of the earliest long wave-length radars were actually antenna arrays of individual radiators positioned and phased to provide a certain antenna pattern [24]; however, it wasn't until World War II that radar technology was proven out to be critically advantageous as an early warning detection system. The state-of-the-art radar systems of the day were large reflect antennas which were mechanically steered to scan a volume. The SCR-270, shown in Fig. 7, was one of the first radars pioneered for early warning detection used by the United States Army in Pearl Harbor during World War II [10]. The main downside of these systems are the slow steering rate and mechanical reliability due to the single point of failure.

While radar is still fundamental to the military target search and track application, it has grown to be fundamental for remote sensing in general where direct human observation is limited, impractical, and/or hazardous. Radar remote sensing is used in a plethora of applications such as: meteorological monitoring, Earth sciences, industrial monitoring, automotive guidance, flight control, and geological surveying. The tremendous growth in radar remote sensing applications has also demanded an evolution of radar from the traditional mechanically steered system to a more robust, reliable, and faster volume scanning system.

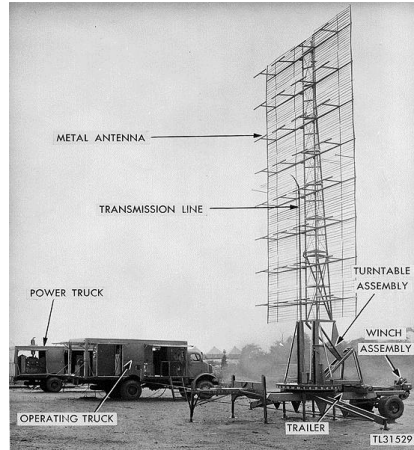


Figure 7: The US Army's SCR-270 radar setup in Pearl Harbor, HI [6]

2.2 *Passive Electronically Scanned Array*

The Passive Electronically Scanned Array (PESA) was the first development of electronic beam steering for a mechanically fixed antenna. In these systems, many smaller antenna elements with an omni-directional characteristic combine in free-space to form an effective wavefront, which is electronically steered by phase shifters behind each of the antenna elements. In the PESA, the transmitter and receiver is common to all antenna elements. The benefit of such a system is that there is no reliance on a mechanically steered structure for scanning, and it has improved scanning rates for a given volume as compared to the mechanically steered radar. The downsides of the PESA are the unrecoverable losses from the phase shifters, the large power levels that the transmitter must generate, and the large power levels that the passives have to tolerate due to the losses associated with having a centralized transmitter – all of which can limit the performance of a PESA in terms of dynamic range. However, these factors do not preclude the use of a PESA, as the architecture can allow for a low-cost electronically scanned array with respect to an AESA. Some of the more famous examples of PESA's include Raytheon's Cobra Dane (1976) and Patriot radars (1975) which are shown in Fig. 8.



(a) Raytheon's Cobra Dane [23]

(b) Raytheon's Patriot radar [30]

Figure 8: Examples of PESA radars

2.3 *Active Electronically Scanned Array*

The first transmit-receive modules arose out the Molecular Electronics for Radar Applications (MERA) program which was developed by Texas Instruments and sponsored by the United States Air Force in 1967 [9]. It was a revolutionary X-band AESA with 604 transmit-receive modules developed using thin-film hybrid microwave integrated circuits (MIC) with silicon transistors on Al_2O_3 (Alumina) substrates. Silicon transistors had just become available in 1964 with very modest output power at 2 GHz and chirped pulse compression was still state-of-the-art, so it was a truly pioneering solution which pushed the limits of both radar and semiconductor technology at the time. The transmit-receive module was a split-module with the top-side of the module including the transmitter, multiplier, and receiver as shown in Fig. 9. The bottom-side of the module contains the phase shifter and local oscillator.

The first AESA to be actually deployed was PAVE PAWS, which was developed by Raytheon in the 1970's as a ballistic missile early warning system and for tracking Earth-orbiting satellites for the United States Air Force Space Command. It has two phased array faces as shown in Fig. 10, each with 1796 hybrid MIC transmit-receive modules which contain four 100 watt discrete packaged silicon transistors operating at UHF. Each transmit-receive module cost \$2000 and has to be liquid cooled on cold plates. Impressively, it is still in operation today [10].

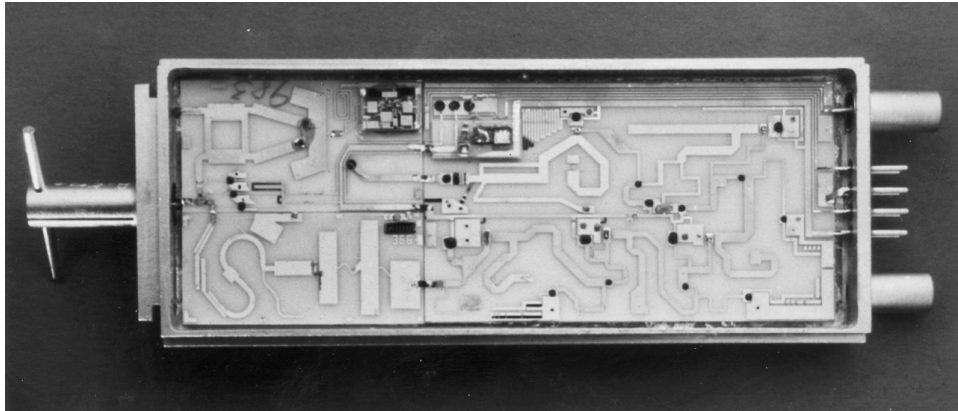


Figure 9: TI's MERA transmitter, multiplier, and receiver module [9]



Figure 10: PAVE PAWS at Clear Air Force Station, Alaska [31]

AESA's dramatically improve the dynamic range performance over PESA's by incorporating transmitters and receivers with phase shifters, i.e. the transmit-receive module, behind every antenna element. The benefits of an AESA are the losses between the amplifiers and antenna elements are reduced considerably, the phase noise of each element becomes uncorrelated, and the individual power amplifier output power requirement is reduced roughly by $10 \times \log(N)$ dB, where N is the number of elements. An additional benefit of the AESA is that individual module failures gracefully degrade the radar's performance as opposed to catastrophic failures of the radar such as in the cases of the PESA and mechanically-steered radars due to their centralized transmitter-receiver. However, the fundamental challenges of the AESA are reducing the cost of the individual transmit-receive modules and fitting the electronics within the lattice spacing required of a large phased array – typically $\lambda/2$ to avoid grating lobes which occur at the maximum steering angle of a phased array. In fact, the push from UHF to L-band frequencies for large AESA's necessitated a move from the use of thin-film hybrid MIC's to monolithic microwave integrated circuits (MMIC) to reduce the size of the circuits in order to cost-effectively fit within the lattice spacing requirement [10].

2.4 Transmit-Receive Module

The block diagram of a modern transmit-receive module is shown in Fig. 11. The typical MMIC's that form the front-end are the transmit-receive switch or circulator, the power amplifier (PA), and the low-noise amplifier (LNA). The back-end, which performs the phase and amplitude control, is often referred to as the common-leg circuit (CLC), as it is a common-leg to both the transmit and receive paths, and it is oriented in such a way that the multi-bit phase shifters, multi-bit attenuators, and amplifiers which comprise the CLC need not be bidirectional through the use of single-pole double-throw switches.

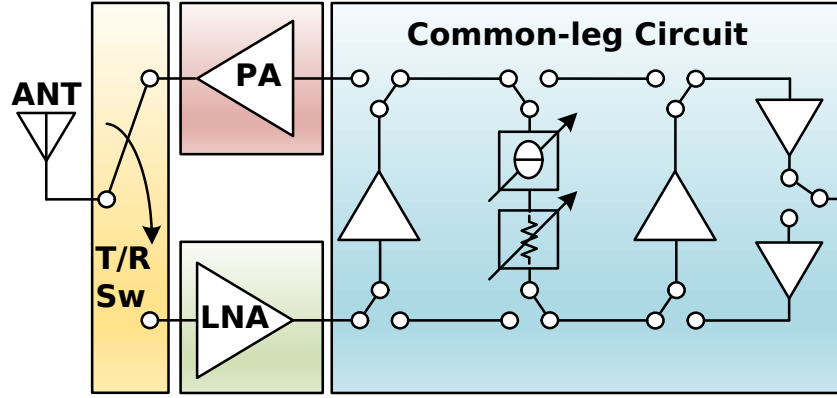


Figure 11: Block diagram of a typical transmit-receive module with shared common-leg circuitry

The transmit-receive switch must switch the mode of the module between the transmitter and the receiver with negligible leakage of signal into the unintended path, oftentimes it must perform this duty quickly for close ranged targets due to the time of flight. Ideally, the switch can handle the large-signal output of the transmitter without compressing and is low-loss such that both the output power of the transmitter and noise figure of the receiver are not compromised.

The low-noise amplifier must amplify the return signal with minimal noise contribution, and it must have high enough amplification such that the noise contribution from subsequent circuit blocks mask the return signal. Survivability to high levels of input power with minimal performance degradation is often a necessary requirement of this circuit block. While conditions causing a full reflection of the transmitter signal back into the receiver are rare, a single event can cause the receivers to be irreversibly damaged. Oftentimes, limiters are placed prior to the low-noise amplifiers to ensure survivability; however, the downside is a reduction in noise performance of the receiver.

The power amplifier must amplify the signal to be transmitted as much as possible, and since radar modulation schemes are typically simple and slow with respect to the frequency of operation, distortion is not typically a concern. More importantly, high

DC-RF efficiency is desired of a power amplifier without requiring a large input power to drive the power amplifier.

As transmit-receive modules progress to millimeter-wave frequencies, the challenges in the production of transmit-receive modules increasingly become focused on the cost and difficulty in terms of producibility. Although, the circuits are reduced in size in proportion to the wavelength of operation, the free-space lattice spacing requirement at W-band frequencies is on the order of 1.5 millimeters. If the wavelength was scaled by another order of magnitude for a 1 THz phased array, it becomes impractical if not impossible to fit a transmit-receive module within the lattice spacing requirement without revolutionary manufacturing changes. In the case of a millimeter-wave module, incorporating as many circuits together into a fully integrated front-end will be essential to reducing cost and increasing producibility. As such, it is apparent that increased integration is critical to the success of producing a millimeter-wave transmit-receive module for a massively-scaled AESA radar.

CHAPTER 3

W-BAND SINGLE-POLE DOUBLE-THROW SWITCH

3.1 Introduction

Recent developments in sub-100 nm SiGe BiCMOS technology include optimized PIN diodes, creating attractive platforms for implementing fully integrated millimeter-wave front-ends. For either pulsed radar or communications front-ends, a single-pole double-throw (SPDT) switch is an essential component. The loss of the SPDT is critical as it both reduces the transmitters output power as well as contributes to the receivers noise figure. Therefore, reducing loss and improving power handling of the SPDT switch are important factors for increasing the limited dynamic range of typical integrated millimeter-wave systems. This chapter discusses the design and results of a state-of-the-art W-band SPDT switch implemented utilizing p-i-n diodes in IBM's 90 nm SiGe BiCMOS technology (9HP), achieving insertion loss and power handling performance comparable to W-band p-i-n SPDT switches in III-V compound semiconductor technologies.

3.1.1 Single-pole Single-throw

A switch, in the simplest configuration, is single-pole single-throw (SPST), which has two states:

1. A 'thru' state which passes a signal between ports 1 and 2.
2. An 'isolation' state which prevents a signal from propagating between ports 1 and 2.

A block diagram of a generic SPST switch is shown in Fig. 12(a).

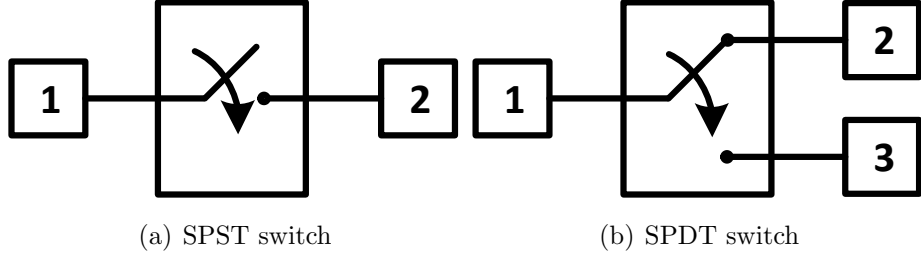


Figure 12: Block diagrams of SPST and SPDT switch configurations

3.1.2 Single-pole Double-throw

A useful switch configuration for transmit-receive modules is the single-pole double-throw (SPDT) configuration. This SPDT switch configuration has a port common to two paths, each comprised of a SPST switch. The SPDT switch has two operating states:

1. A state which passes a signal through between ports 1 and 2 while preventing a signal from propagating between ports 1 and 3.
2. A state which passes a signal through between ports 1 and 3 while preventing a signal from propagating between ports 1 and 2.

A block diagram of a generic SPDT switch is shown in Fig. 12(b). For a transmit-receive switch, the common port is typically connected to an antenna which is shared between a power amplifier and a low-noise amplifier. While many SPDT switches have identical SPST paths, the differences in purposes of each path of a transmit-receive switch do not necessitate a symmetric design. The power amplifier path may emphasize power handling, and the low-noise amplifier path may emphasize insertion loss depending on the tradeoffs for the technology used to implement the switch. Regardless, it is important in the design of a SPDT switch to consider that the performance of the SPST path in the isolation state directly impacts the performance of the other SPST path in the insertion loss state.

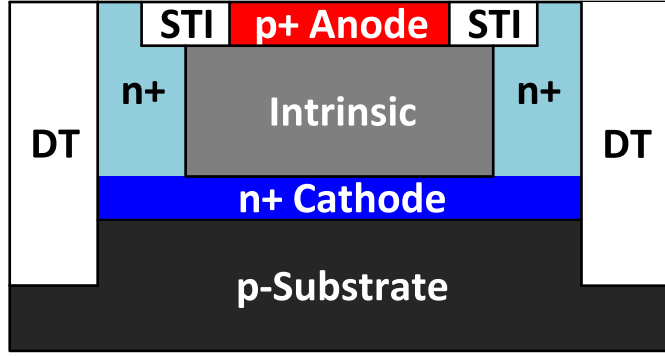


Figure 13: Cross-sectional diagram of a vertical p-i-n diode in a SiGe BiCMOS technology

3.2 Design of a W-band Single-pole Double-throw Switch

3.2.1 p-i-n Diodes

The p-i-n diodes in IBM 9HP are targeted for operation at 60 and 77 GHz, as described in [16, 17]. The p+ anode is formed by the extrinsic SiGe HBT base epitaxial film, the intrinsic region is formed by silicon epitaxial growth, and the cathode is formed by a deep n+ implant with an n+ reach-through to contact the cathode, as shown in Fig. 2 [16]. Typically, the HBT sub-collector is used as the n+ cathode to reduce cost; however, due to the shrinking distance between the base epitaxial film and sub-collector of state-of-art HBTs, this results in high anode-cathode capacitance [17]. Thus, in the present case, the formation of the p-i-n diodes deep n+ implant is decoupled from the HBTs sub-collector to reduce the intrinsic capacitance and improve the performance at mm-wave frequencies.

3.2.2 SPDT Topology

Due to non-negligible device parasitics at millimeter-wave frequencies, there are a limited number of topologies to be considered for a switch. The series-shunt switch topology, which is popular at lower frequencies, uses a series device followed by a shunt device as the switching mechanism. In the isolation state, the series device is turned off, and the shunt device is turned on such that the fraction of the signal that feeds

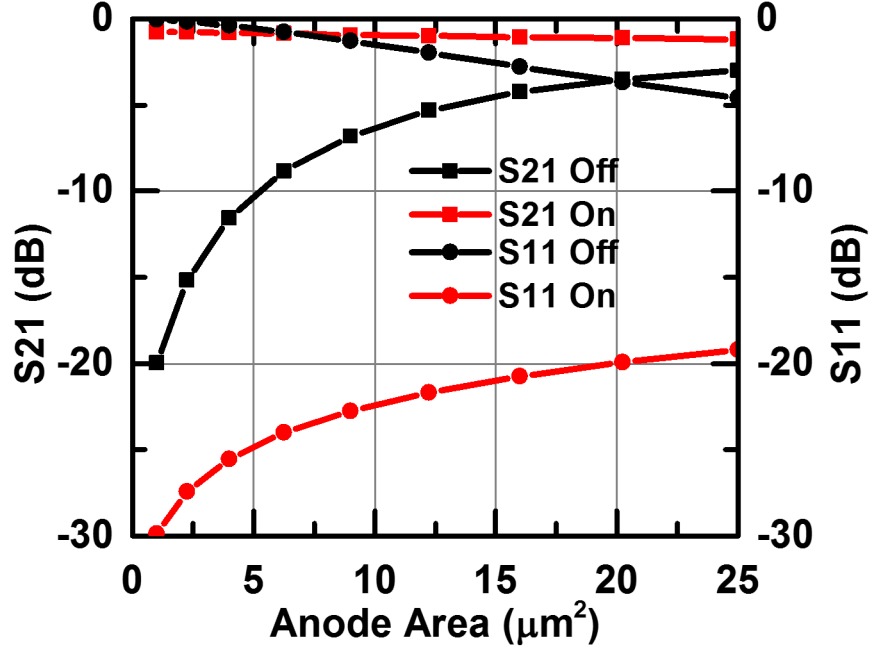


Figure 14: Series p-i-n diode on- and off-state S-parameters over anode area at 94 GHz and V_{ac} of 1 V

through the high resistance of the off-state series device sees a low-resistance path to ground. In the thru state, the series device is turned on, and the shunt device is turned off such that the majority of the signal that passes through the low resistance of the on-state series device sees a low shunt capacitance from the off-state device in parallel with the load impedance. However, at millimeter-wave frequencies the parasitics of the series devices have an impact on the performance of the series-shunt topology. Namely, the on-state series resistance as well as the off-state feedthrough capacitance can be large enough to eliminate the benefit of having the series device.

An evaluation of the series and shunt configuration p-i-n diode S-parameter performance at 94 GHz with a anode-cathode bias, V_{ac} , of 1 V are shown in Figs. 14 and 15, respectively.

The insertion loss of a series p-i-n diode in the on-state at 94 GHz ranges from 0.76 to 1.18 dB with an off-state return loss of 0.05 to 4.58 dB for anode areas of 1–25

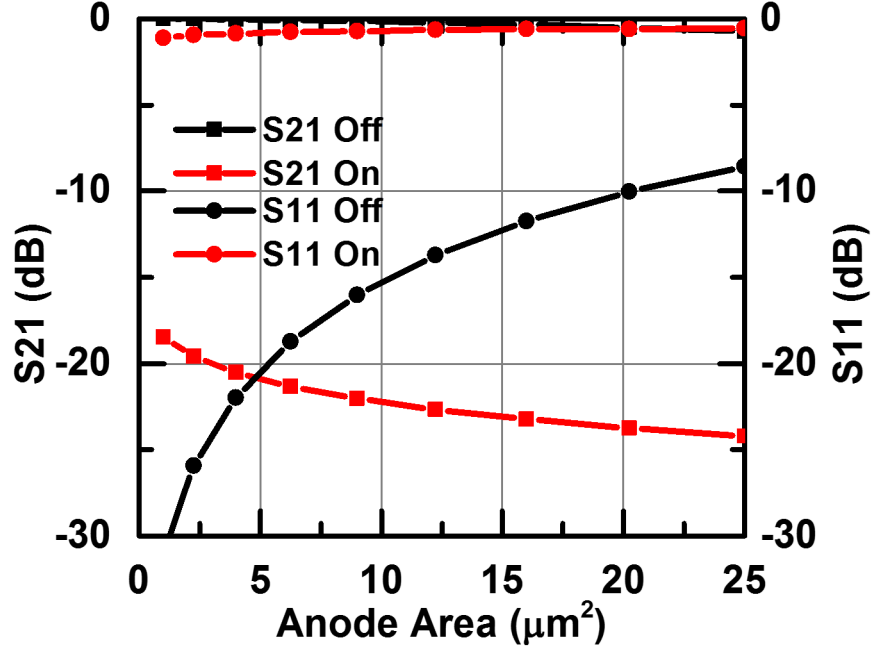


Figure 15: Shunt p-i-n diode on- and off-state S-parameters over anode area at 94 GHz and V_{ac} of 1 V

μm^2 . The insertion loss of the shunt p-i-n diode in the off-state at 94 GHz ranges from 0.01 to 0.74 dB with an on-state return loss of 1.1 to 0.55 dB for anode areas of 1–25 μm^2 . While the series-shunt topology eliminates the need for a quarter-wave ($\lambda/4$) transformer, the insertion loss of a $\lambda/4$ transformer at W-band is only 0.3–0.4 dB. In comparison, the insertion loss contribution from the series device is at least 0.76 dB. In addition, receiver and transmitter circuits often need the spacing created from the quarter-wave transformer which is of reasonable length at millimeter-wave frequencies, eliminating the benefit of a small SPDT switch. For the reasons mentioned, the $\lambda/4$ shunt SPDT switch topology is popular at millimeter-wave frequencies. However, in this topology it is a critical design criteria to maintain high isolation.

For $\lambda/4$ shunt SPDT switch operation, the p-i-n diodes in one arm are turned on, such that they present a short circuit that is transformed to an open at the common port after a $50\ \Omega$ $\lambda/4$ transmission line. The p-i-n diodes in the opposite path are

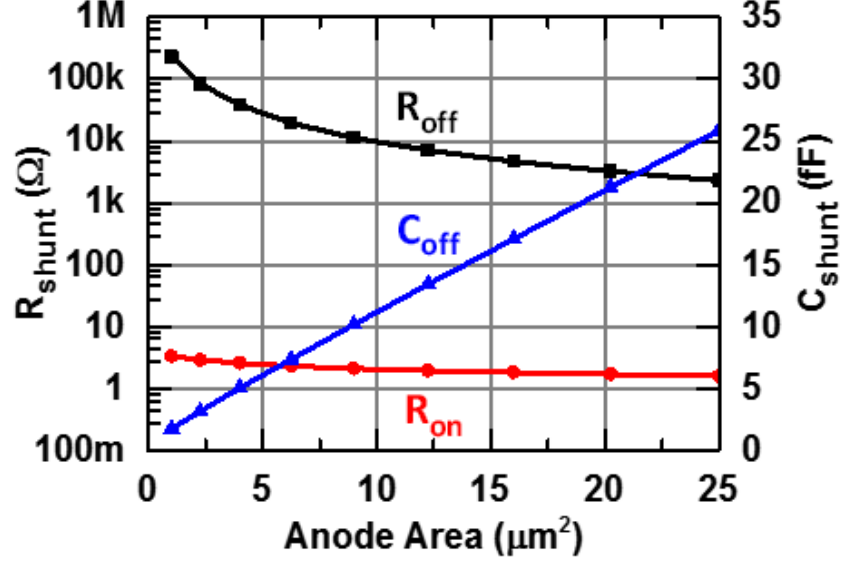


Figure 16: On- and off-state shunt resistance and off-state shunt capacitance over p-i-n diode anode area at 94 GHz

turned off such that the input impedance, Z_{in} , seen from the common port is 50Ω .

Reducing the on-state resistance and increasing the off-state resistance while minimizing the off-state shunt capacitance of the shunt p-i-n diode is essential in order to both maximize the reflection of the isolation path and to minimize the insertion loss over a wide bandwidth. Small devices have high on-state resistance, which leads to a deviation from a perfect short, resulting in poor isolation and increased insertion loss. Larger devices, on the other hand, have a low off-state resistance and an increased off-state capacitance, which increases the insertion loss and reduces the bandwidth of the SPDT switch. The shunt p-i-n device sizing trade-offs are further illustrated in Fig. 16.

The high ratio between $R_{\text{Shunt-off}}$ and $R_{\text{Shunt-on}}$ of the p-i-n diodes, as compared to CMOS and SiGe HBTs for a reasonable anode area, allows for attaining unprecedented performances; however, careful attention needs to be paid to the layout of the devices such that the isolation is not compromised. In order to maximize the isolation using only a single shunt section per arm of the SPDT switch, the via

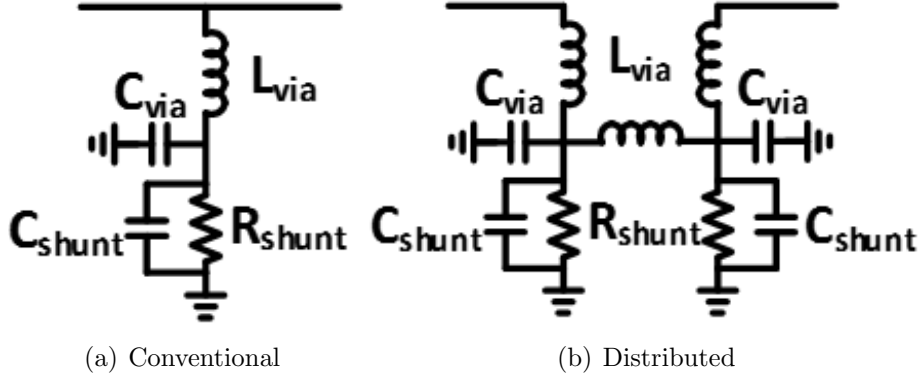


Figure 17: p-i-n diode equivalent models including via parasitics

and interconnect parasitics were incorporated into the transmission line in a similar fashion as Tsai et. al, such that the isolation does not degrade as significantly over frequency due to the imaginary impedance presented by the via interconnects of the p-i-n diodes [28]. This approach is shown in Fig. 17(a) and compared with the conventional approach in Fig. 17(b). The difference between the two methods is clear when looking at Z_{in} of the shunt path of the conventional approach versus Z_{in} of the shunt path of the distributed approach, ignoring the small series inductance between the two distributed devices. The distributed approach bypasses the series via inductance of the device interconnect for a reduced imaginary component of Z_{in} over frequency as compared to the conventional approach.

3.2.3 Generalized Design Procedure

The SPDT switch was designed using the following set of design procedures for a $\lambda/4$ shunt SPDT switch.

1. Size the shunt devices for maximum reflection in the on-state, i.e. minimize R_{on} for minimizing insertion loss and maximizing isolation.
2. Size the shunt devices for minimal shunt conductance in the off-state, i.e. maximize R_{off} for minimizing insertion loss.

3. Size the shunt devices for minimal shunt capacitance in the off-state, i.e. minimize C_{off} for maximizing bandwidth.
4. Minimize the series inductance leading to the shunt devices by integrating the device interconnects in series with the transmission line rather than in shunt.
5. Resonate the off-state shunt capacitance of the devices as well as the interconnects using the shorted stub, TL_{shunt} .
6. Connect the two SPST switch paths with low-loss $50\ \Omega\ \lambda/4$ transmission lines.
7. DC block the SPST paths using series self-resonant MIM capacitors.

One of the ports of the SPDT switch is terminated on-chip with a $50\ \Omega$ TaN resistor to facilitate on-chip measurement. Finally, to allow the use of negative biasing for high power handling in the off-state, TaN resistors are used instead of n-well connections in order to provide discharge paths for some of the MIM capacitors to prevent dielectric breakdown during fabrication. The reason being, are that n-well connections form pn junctions which will be forward biased when a negative bias is applied to the n-well, assuming that the substrate is at ground potential.

3.3 Measurement Results

The schematic and chip micrograph of the W-band SPDT switch are shown in Fig. 18. The chip occupies an area of $580 \times 240\ \mu\text{m}^2$ not including GSG or DC pads.

The S-parameters were measured from 0.05–110 GHz using an Anritsu ME7808C vector network analyzer (VNA) with mm-wave extenders and 1-mm coax probes, and also measured from 110–170 GHz using an Agilent E8364B VNA with OML D-band extenders and WR-6 waveguide probes. Both measurements utilized a probe-tip line-reflect(open)-reflect(short)-match (LRRM) calibration.

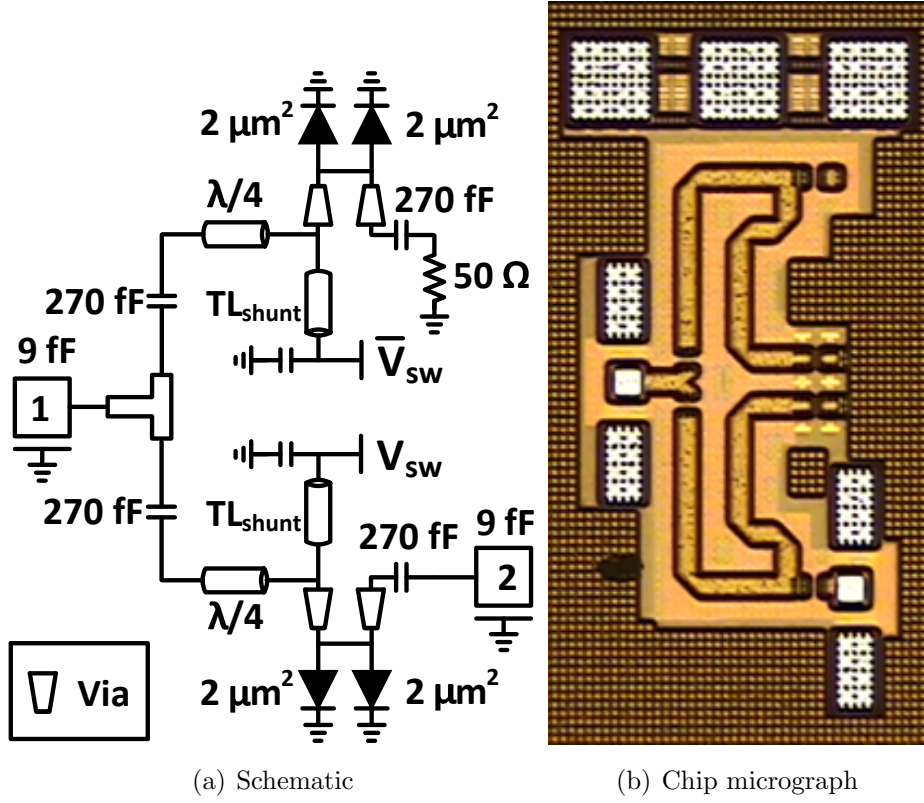


Figure 18: Schematic and chip micrograph of the W-band SPDT switch

The simulated and measured S-parameters of the SPDT switch are shown in Figs. 19 and 20. The RF pads were not de-embedded from the S-parameter measurements, but given a typical Copper-Beryllium (BeCu) probe tip to Aluminum pad contact resistance of 1–2 Ω as shown in [32], this results in a total insertion loss contribution of 0.17–0.34 dB.

The bias voltages for the thru state were $V_{sw} = -4$ V and $\bar{V}_{sw} = 1.2$ V, and vice versa for the isolation state. The DC power consumption of the SPDT switch with one arm in the on-state is 10.2 mW at 1.2 V.

The SPDT achieves a minimum insertion loss of 1.4 dB at 95 GHz with less than 2 dB insertion loss from 73–133 GHz. A maximum isolation of 22.2 dB is achieved at 100 GHz with greater than 20 dB isolation from 79–129 GHz. Input return loss is greater than 10 dB from 73–137 GHz, and output return loss is greater than 10 dB from 73–133 GHz. After considering the aluminum pad contact resistances, the

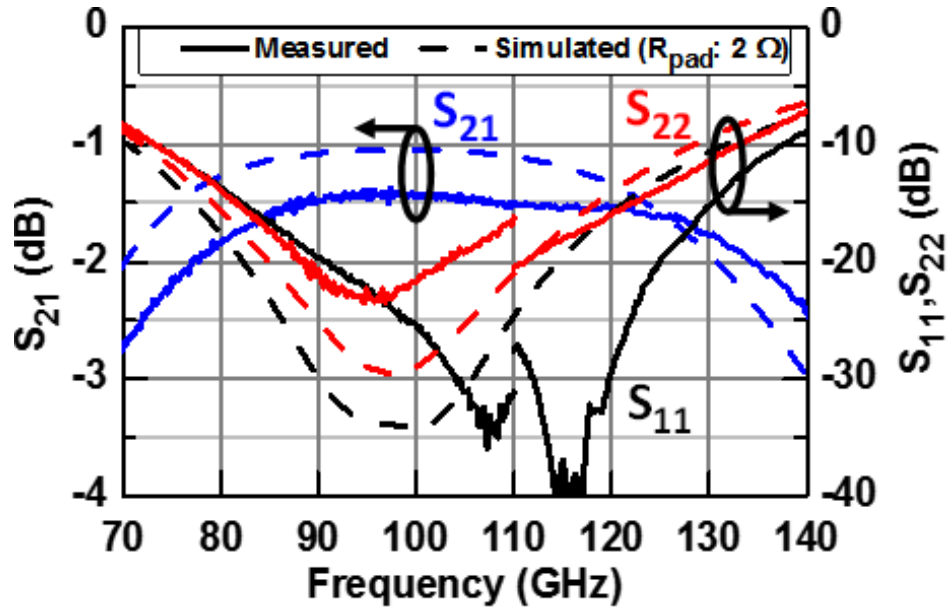


Figure 19: Measured versus simulated S-parameters of SPDT switch in the thru state

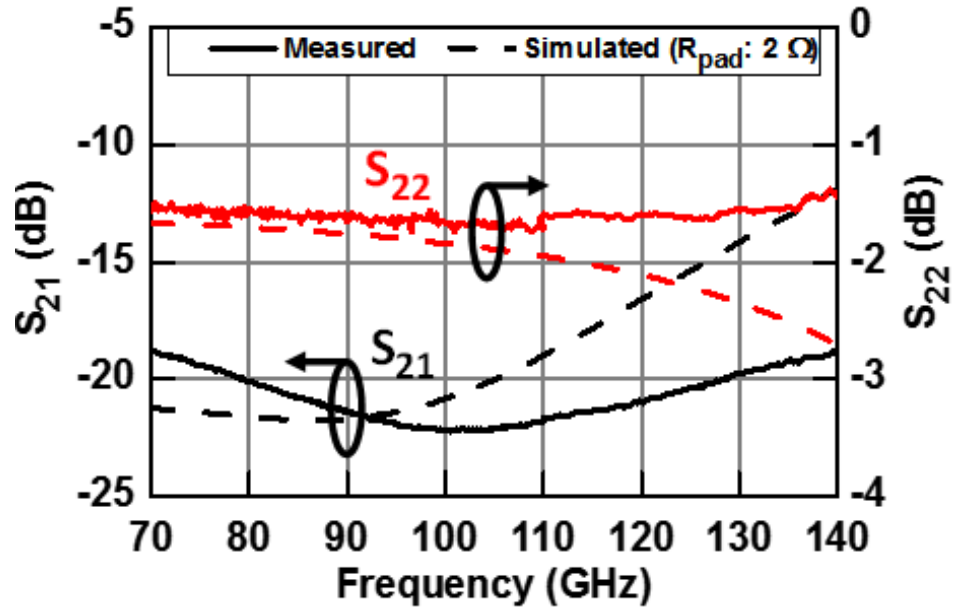


Figure 20: Measured versus simulated s-parameters of SPDT switch in the isolation state

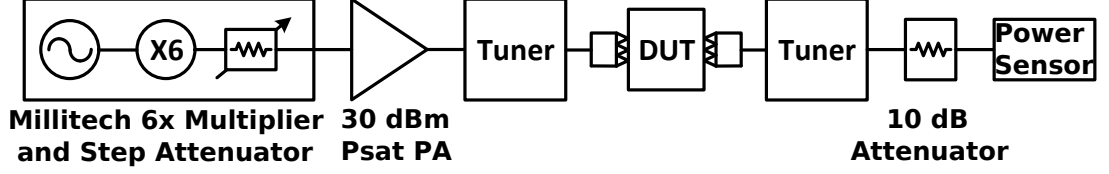


Figure 21: Measurement setup for large-signal characterization at W-band

simulated insertion loss lines up more closely with the measured result. The remaining differences may be attributed to inaccuracies in the initial PIN diode device model and reduced Q-factor of device interconnects as compared to EM simulations.

The large-signal measurements were performed with assistance at Raytheon Integrated Defense Systems in Andover, MA. The W-band large-signal setup consisted of a Millitech 6x multiplier and mechanical step attenuator, a Quinstar 90–96 GHz 1 W power amplifier, Maury WR-10 tuners, a fixed 10 dB attenuator, a HP WR-10 power sensor, and GGB WR-10 waveguide probes as shown in Fig. 21.

The large-signal behavior was measured with the tuners set to present $50\ \Omega$ to the DUT at 92 GHz, where the instrumentation PA produced a peak output power of +24 dBm at the probe tip. The input power was fed to port 2, and the output power was measured at port 1 of Fig. 18(a). This bypasses the loss of the quarter-wave section to report P_{1dB} in a more accurate form for front-end modules. The measured large-signal results are shown in Fig. 21.

Due to the lack of a reverse breakdown in the preliminary p-i-n diode model, the power handling of the thru state was initially estimated through hand calculations. The negative RF voltage swing is limited to the design manual’s specified reverse breakdown of -8.2 V. The positive swing is limited by the turn-on voltage of the diode of about 0.6 V. The DC bias point of V_{sw} is set at the midpoint at -4 V to allow for maximum RF voltage swing. The large-signal operating point of the off-state path of the SPDT is shown in Fig. 22.

Given a $50\ \Omega$ load and a RF voltage swing with a $V_{Peak-Peak}$ of 8.8 V, this results in

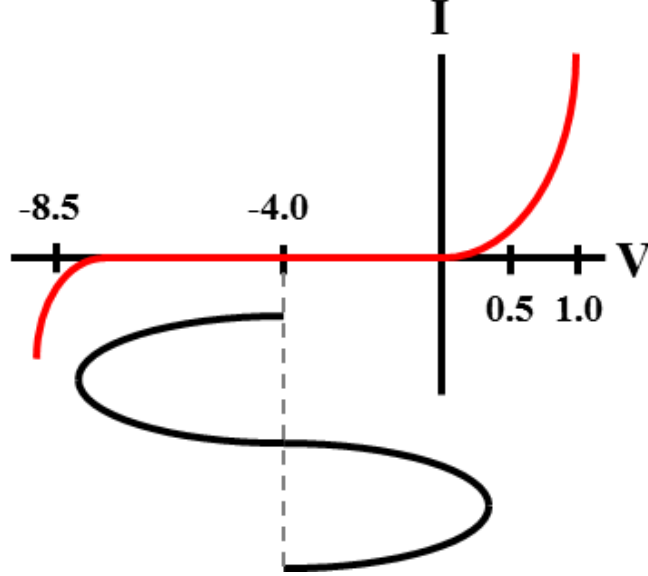


Figure 22: IV characteristic of the thru path of the SPDT showing the large-signal voltage swing headroom for a V_{SW} of -4 V

a maximum linear region of operation of about +23 dBm assuming negligible leakage into the isolation path. This estimate agrees well with the measured results given that the p-i-n diodes are not yet fully conducting at the given voltage extremities.

In Fig. 23, the thru state begins to show signs of compression at +24 dBm, but it did not reach P_{1dB} due to the limited available source power from the measurement setup. While the input tuner does contribute a source of loss which reduces the power available from the instrumentation amplifier, removing it would have also removed the probe mounting position making the measurement impossible.

3.4 Performance Comparison

A comparison of this SPDT switch to other state-of-the-art W-band SPDT switches is shown in Table 1. In comparison to [13], [11], [22], the present work did not de-embed the aluminum RF pads, which would result in an insertion loss reduction of approximately 0.17–0.34 dB. GaAs processes typically use gold as the metallization, and so, they do not have an issue with contact resistance between the metallization

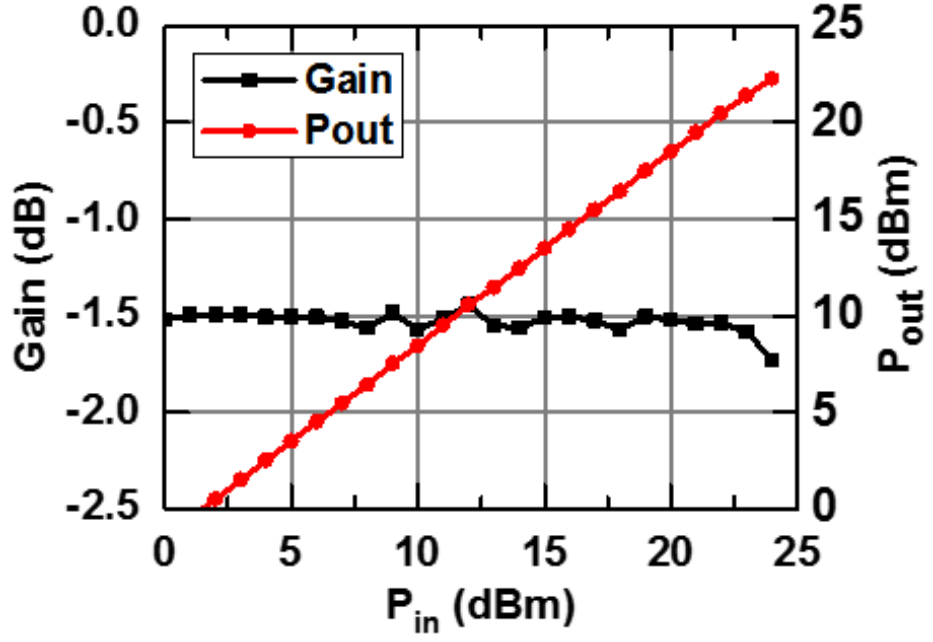


Figure 23: Measured output power and gain across input power of the SPDT switch at 92 GHz

and the probes. The isolation performance is comparable to other SPDT switches except for the series-shunt switch which traded insertion loss for isolation with the topology choice. In comparison to [26], it appears that W-band SPDT switches in silicon-based technologies have finally reached the level of performance which GaAs p-i-n diode SPDT switches attained over a decade ago.

Table 1: Comparison of State-of-the-Art W-band SPDT Switches

Reference	[26]	[13]	[11]	[22]	This Work
Technology	GaAs	130 nm SiGe	130 nm SiGe	90 nm SiGe	90 nm SiGe
Device	p-i-n	nFET	p-i-n	HBT	p-i-n
Topology	$\lambda/4$ shunt	$\lambda/4$ shunt	Series-shunt	$\lambda/4$ shunt	$\lambda/4$ shunt
Frequency (GHz)	75–110	85–105	50–78	77–110	73–133
Insertion Loss (dB)	1.1–1.6	2.3–3.0	2.0–2.7	1.4–2.0	1.4–2.0*
Isolation (dB)	21–22	20–21	25–35	17.5–19	19–22
P_{1dB} (dBm)	–	–	–	19	> 24**
Area (mm ²)	0.94	0.05	0.11	0.14	0.14

* Aluminum RF pad contact resistances have not been de-embedded

** Measurement limited by available source power

CHAPTER 4

W-BAND LOW-NOISE AMPLIFIER

4.1 *Introduction*

One of the most fundamental building blocks of any wireless system is the LNA as its noise figure and gain ultimately determine the minimum sensitivity of the system. With the scaling of SiGe HBTs to sub-100 nm nodes, HBT device optimizations have decreased parasitic base resistance, and therefore, decreased minimum noise figure and increased power gain [16]. This chapter discusses the design and results of a state-of-the-art W-band LNA using 90 nm SiGe HBTs, achieving noise figure performance comparable to W-band low-noise amplifiers in III-V compound semiconductor technologies.

4.1.1 Noise in Cascaded Systems

When designing the receiver path of a transmit-receive module, it is important to understand how the overall noise figure is affected by system parameters. Friis's Equation describes how the total cascaded noise factor of a system relates to the individual noise factor and gain of each of the cascaded stages [7]. From Friis's equation, it is apparent that the noise factor of the first stage contribution dominates the overall noise figure, and the noise factor contributions of subsequent stages are reduced by the gain of the previous stages.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_n}, \quad (3)$$

where F_{total} is the total cascaded noise factor, F_n is the noise factor of stage n, G_n is the gain of stage n, and the noise figure is related to noise factor by $NF = 10 \times \log(F)$ in dB.

Friis's equation is useful for receiver design both at the system design level and at the low-noise amplifier design level. The first block of the system, the transmit-receive switch, is typically a lossy circuit. Therefore, it must be designed to contribute as little insertion loss as possible to the receive path as this loss contributes directly to the overall noise figure. Following the SPDT switch, the low-noise amplifier should be designed for minimum noise figure and at least 20 dB gain in order to reduce the noise contribution from subsequent stages by at least 2 orders of magnitude. The LNA design focuses both on minimizing noise figure and maximizing gain from the first and/or second stage. Subsequent stages of the LNA, if required, emphasize boosting gain if the gain per stage of the LNA is insufficient such that the impact of noise figure from subsequent switches, phase shifters, step attenuators, and/or mixers is insignificant when divided out by the gain of the LNA.

4.1.2 Noise Figure Measurement

The Y-factor method was used to characterize the noise figure of the LNA using a noise source, a block downconverter, and a noise figure analyzer (NFA). A noise source, containing a diode, requires a characterization of the two states of noise temperatures: on (in reverse-breakdown) or off. Noise sources are always provided with an Excess Noise Ratio (ENR) table over the frequency range of use, where the ENR is defined as the difference between the two diode state temperatures normalized to a reference temperature of 290 K.

$$ENR_{dB} = 10 \times \log \frac{T_s^{ON} - T_s^{OFF}}{T_o}, \quad (4)$$

where T_s^{ON} is the noise temperature when the noise source diode is in reverse breakdown, T_s^{OFF} is the noise temperature when the noise source diode is off, and T_o is the reference temperature of 290K.

Once the ENR table is known, the Y-factor of the system must be determined with a noise figure calibration. The Y-factor is defined as the ratio of two noise power

levels or two noise temperatures, one measured with the noise source diode on versus and one measured with the noise source diode off. The system-level Y-factor must be determined without the DUT or input fixture. This is performed at the interface where the ENR table is defined, which is at the waveguide interface in the case of the W-band noise source. Then, a loss table of the input probe fixture over frequency is added into the NFA. The system at this point has a noise power measured at the NFA and a traceable relationship of that measured noise power back to the noise power of the source in the on and off states. Any subsequent noise power which is added to the system at the NFA, for example the noise contribution from the DUT, can be easily determined at this point. The Y-factor method of noise figure measurement is described in detail in Agilent's Application Note 57-2 [1].

A caveat of noise figure measurements at millimeter-wave frequencies are that they invariably have high associated uncertainties with the main sources of uncertainty originating from the noise source itself and from deembedding the loss of the input probe. In addition, care needs to be taken in order to minimize the errors that arise from the changing waveguide reference planes during calibration and deembedding.

4.2 Design of a W-band Low-noise Amplifier

4.2.1 Generalized Design Procedure

The LNA was designed using the following set of design procedures for minimizing noise figure, maximizing gain, and maximizing matching bandwidth of a LNA.

1. For a given device size, find an optimum current bias, I_C , for minimum noise figure without trading off too much gain.
2. Size the HBT emitter length, L_E , for wideband, simultaneous noise and input matching. Typically, additional inductive emitter degeneration is required to accomplish this.

3. The emitter degeneration inductor is sized to match the real portion of the input impedance, R_{in} , of the HBT with the tradeoff of reduced gain using series-series negative feedback. As a result, the emitter degeneration helps to ensure that the transistor will be unconditionally stable in-band.
4. Due to the relatively low gain per transistor at millimeter-wave frequencies, multiple stages must be utilized to reduce the influence on noise figure of subsequent components in the receiver as determined by the Friis equation. Typically, a gain of 20 dB or greater is sufficient.
5. The input stages are designed to have minimum noise figure with wideband input matching, the intermediate stages are designed for maximum gain, and the output stage is designed as a buffer to have wideband output matching.
6. The out-of-band instabilities are taken care of with the the sizing of the input and output biasing shorted stub lengths of each stage.

The device sizing and current biasing was first evaluated for minimum noise figure, maximum gain, and ease of matching over a wide bandwidth. A nominal bias current of 0.65 mA/ μm at a collector-emitter voltage of 1.2 V was first chosen as a tradeoff between minimum noise figure, NF_{min} , and maximum available gain, G_{max} . The NF_{min} and G_{max} for inductively emitter degenerated HBT's over frequency versus L_E is shown in Fig. 24. The amount of inductive emitter degeneration was varied to in an effort to match the real part of the input impedance for each device size. The spread in NF_{min} is about 0.5 dB across the band, while the spread in G_{max} is about 1 dB across the band for the L_E range of 1–8 μm . Clearly, NF_{min} isn't affected as much as G_{max} with respect to device size; therefore, the focus is instead placed on sizing for ease of device matching while maintaining high G_{max} .

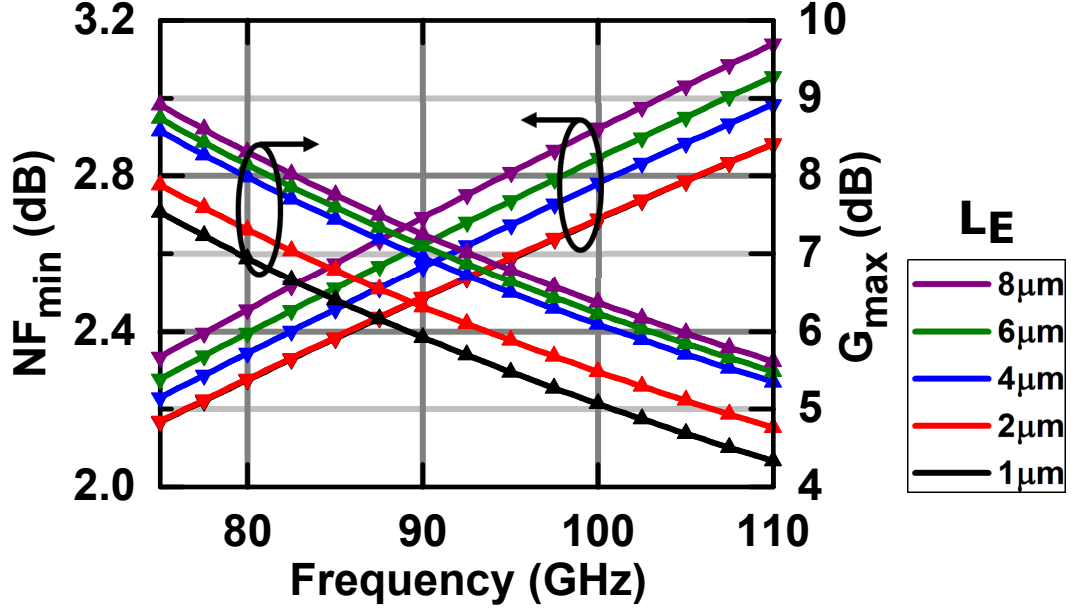


Figure 24: NF_{min} and G_{max} for a common-emitter CBEBC HBT with inductive emitter degeneration at 1.2 V_{CE} and 0.65 mA/ μm I_C from 75–110 GHz vs emitter length, L_E , in IBM 9HP

Simultaneously matching the input reflection coefficient, Γ_{in} , optimum source reflection coefficient, Γ_{opt} , and the output reflection coefficient, Γ_{out} , over a wide bandwidth can be quite difficult. The tradeoffs between Γ_{in} and Γ_{opt} versus device size is illustrated in Fig. 25. An emitter length of 4 μm is selected as a compromise. Inductive emitter degeneration is used to increase R_{in} while sacrificing some gain, enabling unconditional stability and wideband, simultaneous noise and input matching.

4.2.2 LNA Topology

Following the preliminary evaluation of bias current and device sizing with degeneration such that input matching is reasonable, the choice of LNA topology was evaluated between the common-emitter and cascode topologies. The main criteria for evaluation are the overall noise figure, gain, and power supply biasing. Using Friis's cascaded noise equation with G_{max} and NF_{min} , it is determined that there is sufficient gain per stage using emitter degenerated common-emitter stages versus emitter degenerated cascode stages at W-band to maintain a low total noise figure in this

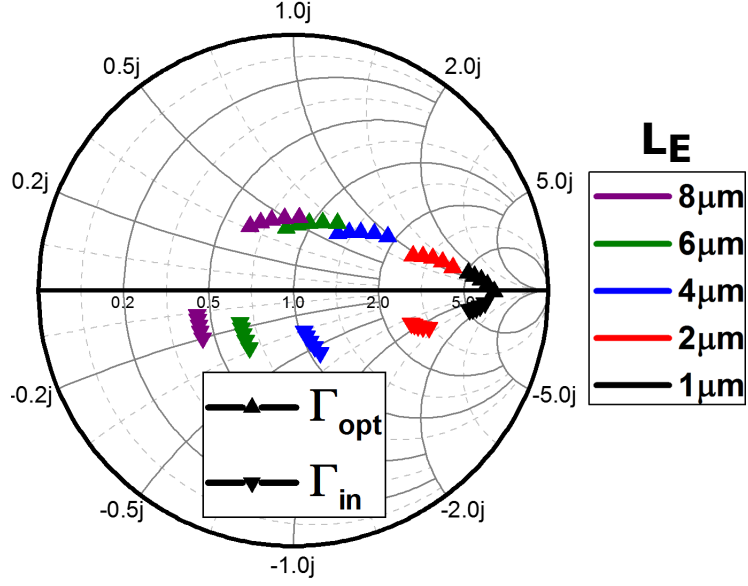


Figure 25: Γ_{in} and Γ_{opt} for a common-emitter CBEBC HBT with inductive emitter degeneration at 1.2 V_{CE} and 0.65 mA/ μm I_C from 75–110 GHz vs L_E in IBM 9HP

technology as shown in Fig. 26(a). In addition, it is observed that while a degenerated cascode stage provides higher overall gain than two degenerated common-emitter stages, the overall noise figure remains higher in the cascode as shown in Fig. 26(b). The common-emitter topology provides lower overall cascaded noise figure at a lower current bias, and in addition, the common-emitter topology reduces the supply voltage required for the LNA and eliminates the additional bias supply on the upper base node of the common-base device. Therefore, a common-emitter topology is chosen for the design of the LNA. Note that this first order analysis using the Friis equation with G_{max} and NF_{min} only works for the case when Γ_{in} and Γ_{opt} can be simultaneously matched.

4.2.3 Matching Networks

The LNA employs a design approach where the first two stages are matched for minimum noise figure, the following two stages are matched for maximum gain above the center frequency, and the final stage serves as buffer to improve the output match. A total of 5 stages were designed such the gain of the LNA was greater than 25 dB

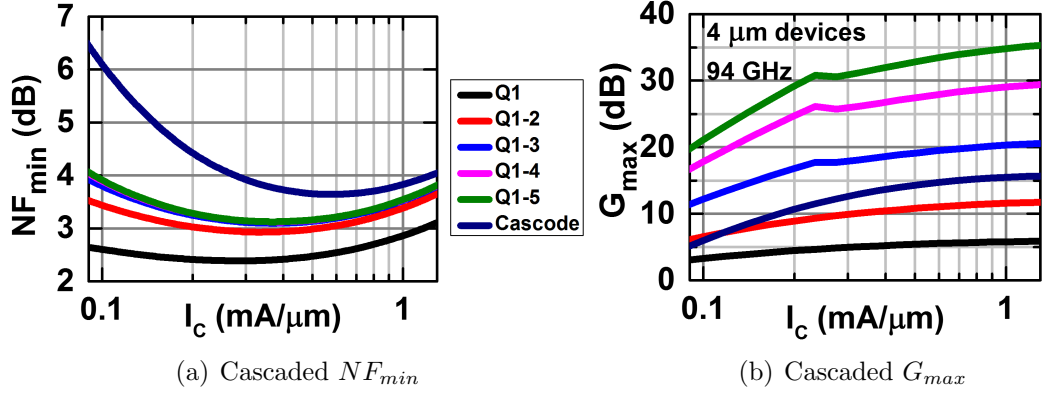


Figure 26: Comparison of cascaded common-emitter stages versus a cascode for 4 μm emitter length devices at 94 GHz at 0.3 V_{CB} and 0.65 mA/ μm I_C

across the band. Input matching is handled primarily by the shunt MSL used for base biasing, since the device size and inductive emitter degeneration were chosen to bring Γ_{in} and Γ_{opt} close to 50 Ω . The matching network for a single stage of the LNA is shown in Fig. 27.

Input matching is handled primarily by the series-resonant DC block MIM capacitor and shunt 75 Ω MSL used for base biasing as the device sizing and inductive emitter degeneration were already chosen to bring the input match close to 50 Ω depending on the stage under consideration. The first and final stages utilize the most inductive emitter degeneration for matching, while the intermediate stages have the least inductive emitter degeneration for in-band stability. The smith chart of the input matching network is shown in Fig. 28(a). Γ_{in} and the reflection coefficient of the source matching network, Γ_S , are conjugates, indicating good input matching. In addition, Γ_{opt} , while slightly rotated in phase from Γ_S , is also in a good location with respect to Γ_{in} , indicating good noise matching. The final input matching network responses of this stage are indicated by Γ_{in1} and Γ_{opt1} .

Output matching of the stage is accomplished with a series 75 Ω MSL and a shunt 75 Ω MSL used for biasing the collector. The smith chart of the output matching network is shown in Fig. 28(b). Γ_{out} and the reflection coefficient of the load matching

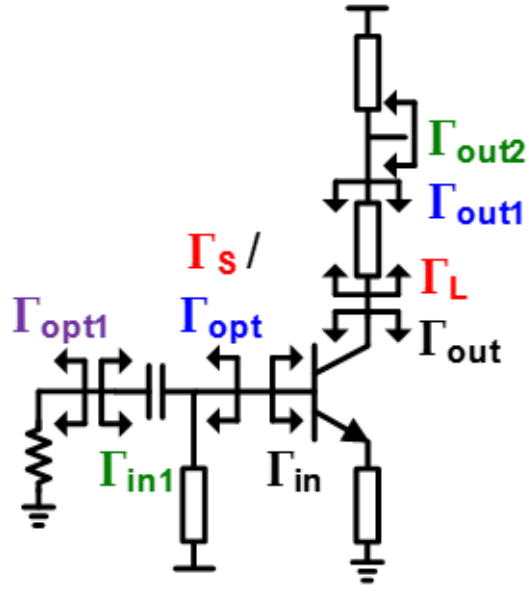


Figure 27: Matching network schematic of a single stage of the LNA

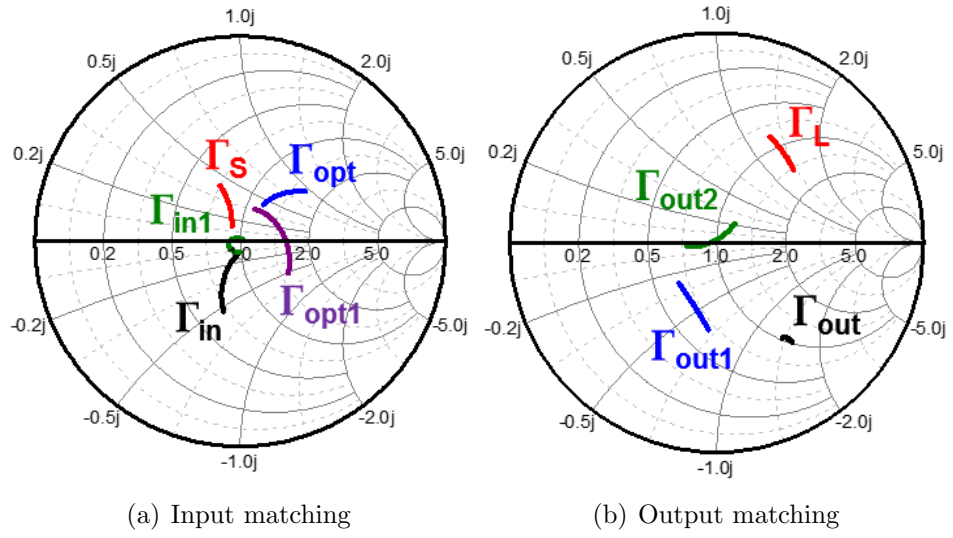


Figure 28: Smith Charts of the matching networks of a single stage of the LNA over 75–110 GHz

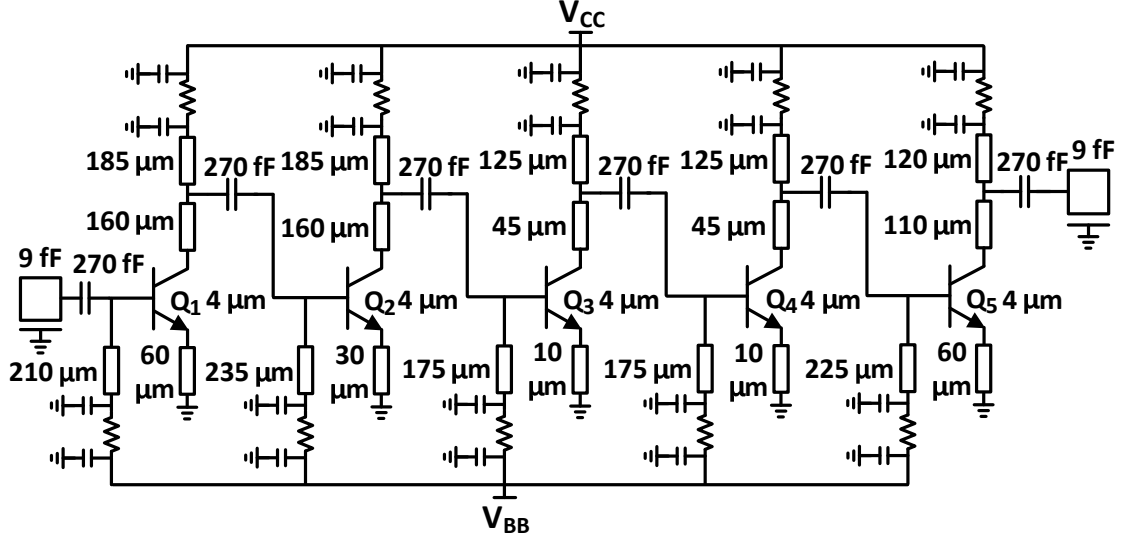


Figure 29: Schematic of the W-band LNA

network, Γ_L , are conjugates, indicating good output matching. The final output matching network response is indicated by Γ_{out2} . Note that the common-emitter topology has finite reverse isolation, so the input and output matching process must be iterated to reach a final solution. This matching network analysis used the final respective source or load matching networks when the input or output was being matched.

The biasing short stubs used for biasing the base and collector nodes were formed by 540 fF of shunt MIM capacitors, a 15 Ω series TaN resistor, and 2 pF of shunt dual MIM capacitors. The series resistor reduces the quality factor of the bias network following the first shunt MIM capacitors such that stage-to-stage feedback through the bias network and self-resonance of the bias network are not concerns for the circuit performance, and 6 pF of bypass capacitance is placed between each DC bias pad to provide additional power supply decoupling.

4.3 Measured Results

The schematic and chip micrograph of the W-band LNA are shown in Figs. 29 and 30. The chip occupies an area of $600 \times 500 \mu\text{m}^2$ not including GSG or DC pads.

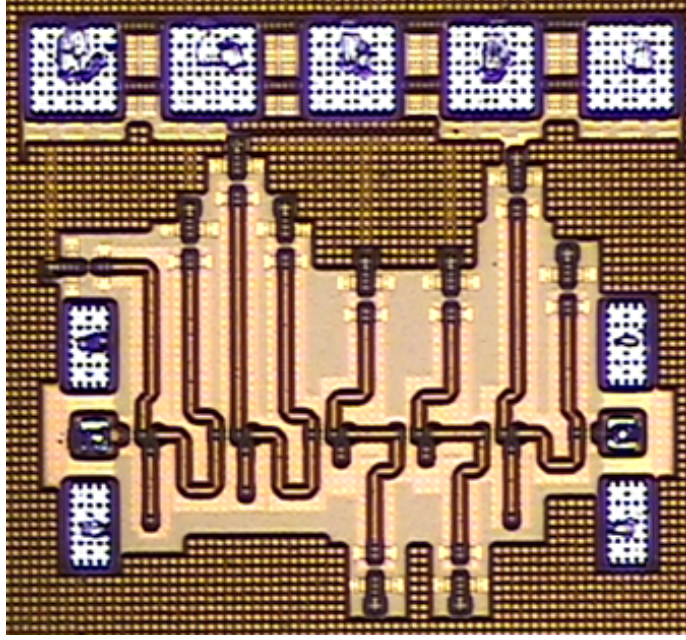


Figure 30: Chip micrograph of the W-band LNA

The S-parameters were measured from 0.05–110 GHz using an Anritsu ME7808C VNA with mm-wave extenders and 1-mm coax probes, and S-parameters were also measured from 110–170 GHz using an Agilent E8563 VNA with OML D-band extenders and WR-6 waveguide GSG probes. Both measurements utilized a probe-tip line-reflect(open)-reflect(short)-match (LRRM) calibration.

The noise figure measurements were performed with assistance at Raytheon Integrated Defense Systems in Andover, MA. The W-band noise figure setup consisted of a Quinstar WR-10 noise source and isolator with a combined average ENR of 15.5 dB, GGB WR-10 waveguide probes, Agilent K88/K98/K99 W-band block downconverters, and an Agilent 8975A noise figure analyzer (NFA) as shown in Fig. 31. The three downconverter blocks cover 75–89, 86–100, and 96–110 GHz, respectively, and contain an isolator and a high pass filter before the mixer for image rejection – essential for making accurate single side band (SSB) Y-factor noise measurements. The measured noise figure is the same with or without NFA calibration once input fixture loss is factored into the ENR table due to the high gain of the DUT.

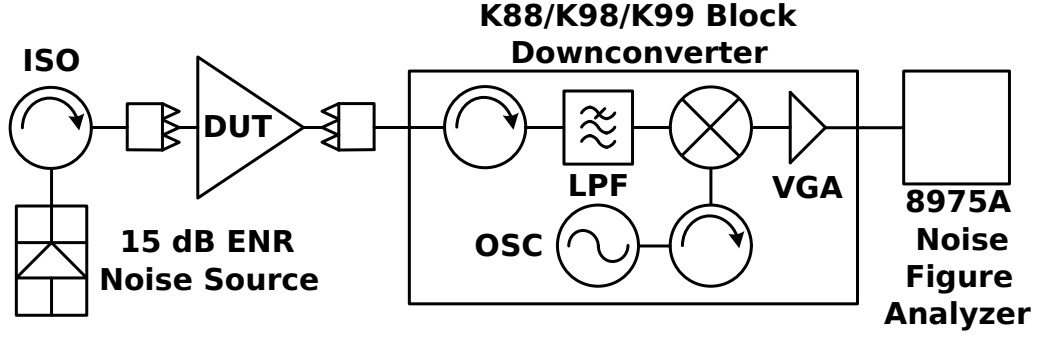


Figure 31: Measurement setup for W-band noise figure

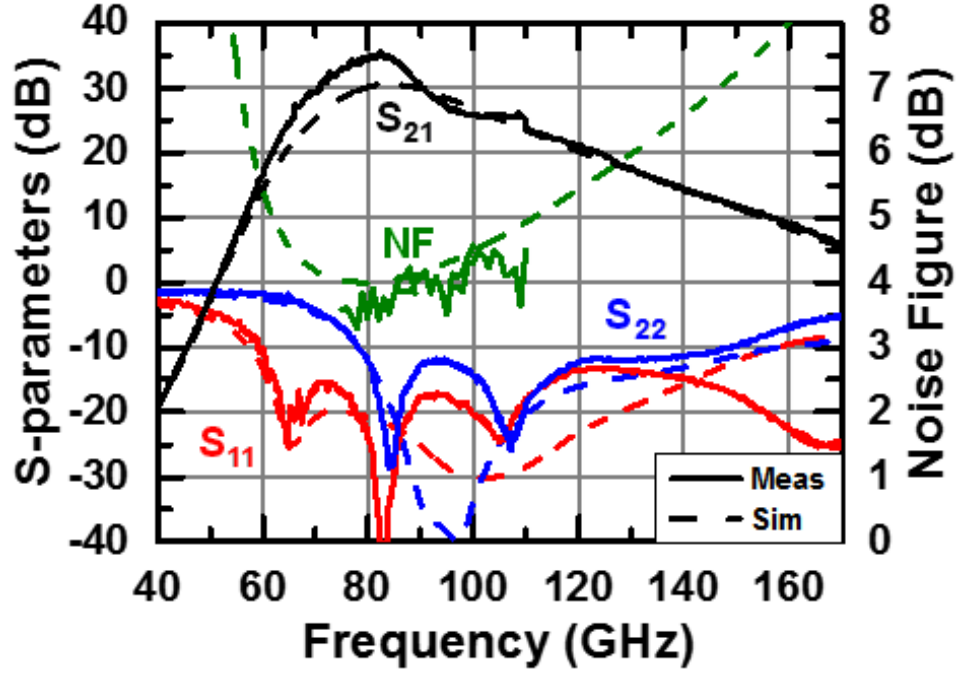


Figure 32: Measured versus simulated s-parameters and noise figure

The measurement results compared to simulation are shown in Figs. 32 and 33. Measurements are performed with a bias of 1.2 V and 13 mA of total collector current (0.65 mA/ μm) unless otherwise noted. The measured S-parameter and noise figure results are generally in good agreement with simulation. The gain peaks at 34.5 dB from 80-82 GHz and levels off to 25 dB by 110 GHz with greater than 25 dB gain achieved across the full W-band. Input return loss is greater than 10 dB from 60-170+ GHz, and output return loss is greater than 10 dB from 78-149 GHz.

The measured noise figure, with relatively large uncertainty, is as low as 3.5 dB

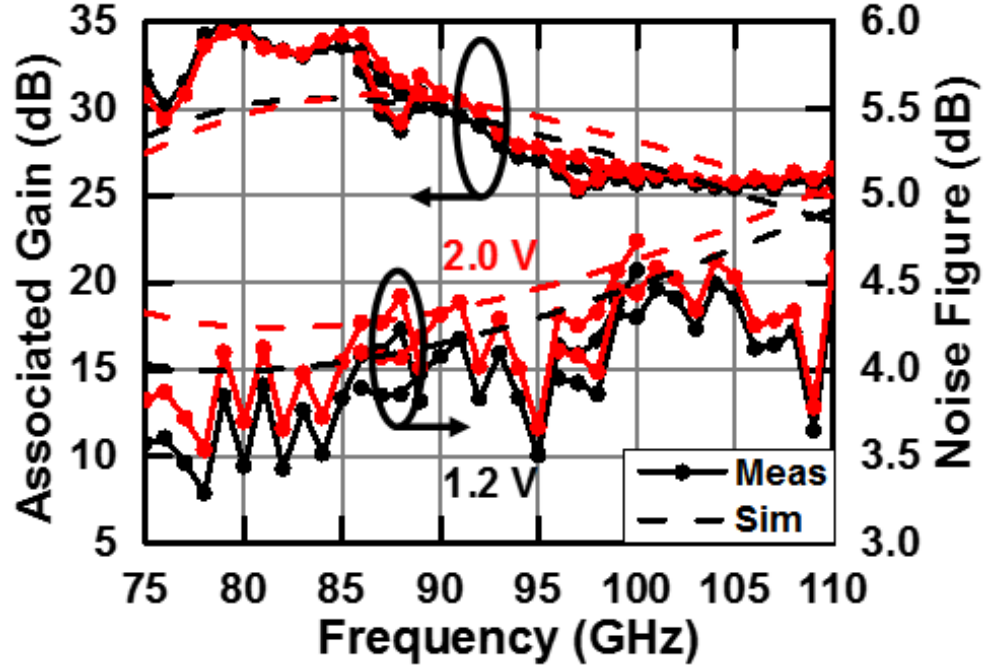


Figure 33: Measured versus simulated noise figure and associated gain versus V_{cc}

below 80 GHz and is below 4.5 dB across the entire W-band. While the measured and simulated noise figure exhibit the same trend across frequency, the measured noise figure is up to 0.5 dB lower than simulated, and corresponds to the frequencies at which the measured gain is higher than simulated. At the frequencies at which the measured gain is close to the simulated gain, the measured noise figure corresponds closely to the simulated value.

The large-signal measurement setup consists of an OML S10MS 6x multiplier, a fixed 20 dB attenuator, a Millitech voltage controlled attenuator, an Agilent WR-10 power sensor, 1-mm coax probes, and HP WR-10 to 1-mm coax converters.

The large-signal behavior was measured at 94 GHz. When biased nominally, the LNA outputs up to +2.5 dBm P_{sat} with an IP_{1dB} of -23 dBm. The measured large-signal results are shown in Fig. 6. For increased dynamic range, the LNA can be biased above BV_{CEO} without catastrophic avalanche breakdown occurring, due to the low DC resistance presented to the base ($< 20 \Omega$) [21]. When biased at 2.0 V, the LNA outputs up to +6.8 dBm P_{sat} with an IP_{1dB} of -21 dBm at 94 GHz. At 2.5 V, the

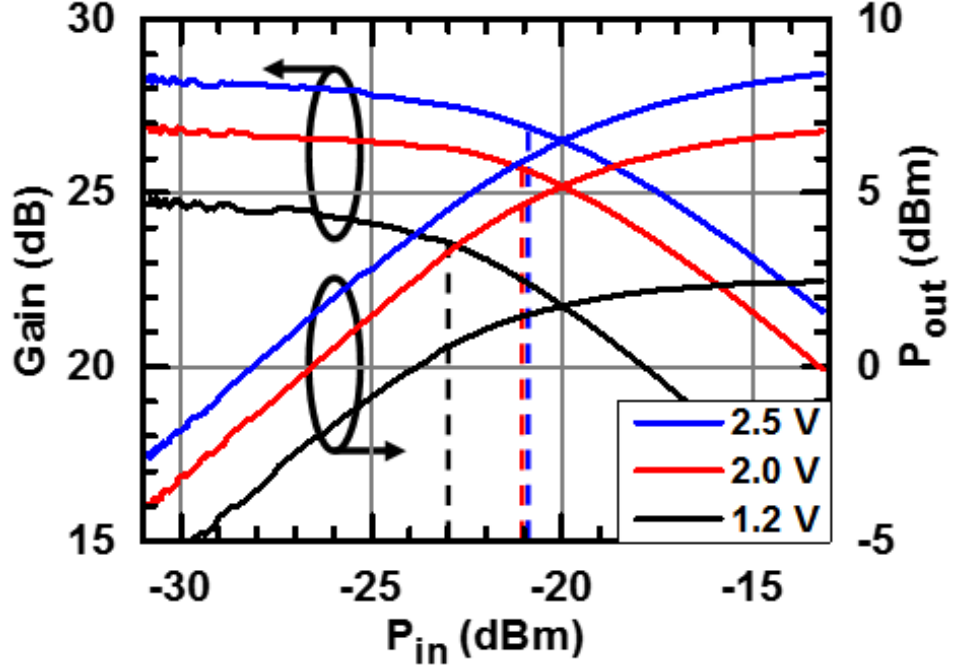


Figure 34: Measured output power and gain across input power at 94 GHz versus V_{cc}

LNA outputs up to +8.5 dBm P_{sat} with an IP_{1dB} of -21 dBm at 94 GHz. However, one caveat of biasing above BV_{CEO} is that impact-ionization begins to induce an excess noise contribution to the noise figure [18], and this effect can be seen in Fig. 33 for a bias voltage of 2.0 V.

Finally, a preliminary evaluation of performance degradation from long term RF stress was performed on the W-band LNA with an input power of +10 dBm (39.2 dB compressed) at 88 GHz for 99 hours. No significant changes were observed other than slight DC offsets caused by the initial burn-in. This is a key survivability test for remote sensing applications where there may be limited isolation from a high power transmitter coupling back into the receiver.

4.4 Performance Comparison

A comparison of this LNA to other state-of-the-art W-band LNAs is shown in Table 2. In comparison to the other W-band LNA also implemented in IBM 9HP

Table 2: Comparison of State-of-the-Art W-band SPDT LNAs

Reference	[12]	[14]	[2]	[29]	[33]	This Work
Technology	50 nm mHEMT	100 nm HEMT	45 nm CMOS	130 nm SiGe	90 nm SiGe	90 nm SiGe
f_T/f_{max} (GHz/GHz)	375 500	230 -	340 -	300 500	300 310	300 350
Topology	2-stg Casc.	3-stg CS	3-stg CS	2-stg Casc	4-stg CE	5-stg CE
Frequency (GHz)	80–100	86–96	95	110	75–105	75–110
Gain (dB)	20	17.5–20	10.7	20.5	17–19	25–34
NF (dB)	1.9	1.9–2.7	6.0	4.0	5.1–8.5	3.5–4.5
P_{DC} (mW)	–	18	52	17	43	15.6
Area (mm ²)	1.13	–	0.32	0.41	0.14	0.30

[33], this work focused on inductive emitter degeneration in conjunction with device sizing which improved input match and noise figure considerably. The mismatch losses and noise match, likely due to inaccurate modelling of parasitics, led to a worse noise performance in [33]. In comparison to [29], this work used a technology with worse f_{max} performance but with a common-emitter topology instead of cascode topology to ultimately achieve a similar level of noise performance. And finally, in comparison to [12] and [14], this work demonstrates that SiGe HBT technology is approaching a level of performance where it can contend with the state-of-the-art noise performance in advanced InGaAs mHEMT technologies.

CHAPTER 5

CONCLUSION

This thesis details the design and results of state-of-the-art W-band circuits implemented in a 90 nm SiGe BiCMOS technology for radar remote sensing applications.

The design and measurement results of a state-of-the-art W-band SPDT switch implemented using p-i-n diodes in a 90 nm SiGe BiCMOS technology was discussed. This work does not de-embed the aluminum RF pads, which would result in an insertion loss reduction of approximately 0.17–0.34 dB. To our best knowledge, this is the lowest insertion loss and highest power handling W-band SPDT switch reported in any silicon-based technology to date.

The design and measurement results of a state-of-the-art W-band LNA implemented in a 90 nm SiGe BiCMOS technology was discussed. The high gain, wide-band matching, and low noise figure of the realized W-band LNA make it immediately useful for many remote sensing applications. To the author's best knowledge, this is the first report of a sub-4 dB noise figure from a W-band LNA in a silicon-based technology.

The performance metrics of the W-band circuits, combined with the high reliability of SiGe technology, demonstrate the potential of SiGe BiCMOS technology for emerging radar remote sensing applications at millimeter-wave frequencies.

5.1 Future Work

The results of this work demonstrate that SiGe HBT's can provide exceptional performance for the critical transmit-receive circuit blocks at millimeter-wave frequencies. Currently, there does not exist a *long-range*, millimeter-wave radar implemented

using silicon-based technologies for performance-related reasons. The W-band performance recently attained from the LNA and SPDT switch circuit designs raise new questions as to whether a long-range, millimeter-wave radar implemented using SiGe BiCMOS technology could in fact be competitive in terms of performance and cost to III-V compound semiconductor technologies. The silicon-based approach would require massive scaling, but with large volumes, reduced integration touch labor, and digital back-end flexibility, a silicon-based approach could begin to be appealing in certain radar remote sensing applications.

The W-band power amplifier is under investigation as it is the primary barrier to entry for demonstration of a W-band transmit-receive module with possibilities to scale to a phased arrays. While large output powers cannot be easily attained with respect to other technologies, achieving high power added efficiency is the one factor that can offset this handicap as free-space combining in large-scale arrays minimizes the loss of efficiency associated with power combining on-chip.

Further investigations of SPDT switch topologies will continue for power handling and isolation improvements with minimal degradation of insertion loss. A low-noise amplifier with built-in power limiting while maintaining sub-4 dB noise figure performance will also be investigated to ensure robust, fail-safe performance when integrated in a transmit-receive module.

The main goal of future work will be to continue individual investigations of the aforementioned circuit blocks as well as their integration into a transmit receive module with amplitude and phase control for eventual W-band phased array system-on-chip demonstration.

REFERENCES

- [1] AGILENT TECHNOLOGIES, “Application note 57-2: Noise figure measurement accuracy – the y-factor method.” <http://cp.literature.agilent.com/litweb/pdf/5952-3706E.pdf>.
- [2] CETINONERI, B., ATESAL, Y., FUNG, A., and REBEIZ, G., “W-band amplifiers with 6-db noise figure and milliwatt-level 170-200-ghz doublers in 45-nm cmos,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 60, pp. 692–701, March 2012.
- [3] COMMITTEE ON EARTH SCIENCE AND APPLICATIONS FROM SPACE: A COMMUNITY ASSESSMENT AND STRATEGY FOR THE FUTURE, NATIONAL RESEARCH COUNCIL, *Earth Science and Applications from Space: National Imperatives for the Next Decade and Beyond*. The National Academies Press, 2007.
- [4] CRESSLER, J. D. and NIU, G., *Silicon-Germanium Heterojunction Bipolar Transistors*. Artech House, 2002.
- [5] DURDEN, S.L., TANELLI, S., EPP, L., JAMNEJAD, V., PEREZ, R., PRATA, A., SAMOSKA, L., LONG, E., FANG, H., ESTEBAN-FERNANDEZ, D., and LEE, C., “A cloud and precipitation radar system concept for the ace mission,” in *Earth Science Technology Forum*, pp. 1–4, 2011.
- [6] FIRST LIEUTENANT HAROLD ZAHL, “Scr-270 radio set.” <http://en.wikipedia.org/wiki/File:SCR-270-set-up.jpg>, September 2006. Radio Set SCR-270 set up for operation. This is the model of portable unit located at Opana point that detected the Pearl Harbor attacking planes 55 minutes prior to the attack.
- [7] FRIIS, H., “Noise figures of radio receivers,” *Proceedings of the IRE*, vol. 32, pp. 419–422, July 1944.
- [8] HEINEMANN, B., BARTH, R., BOLZE, D., DREWS, J., FISCHER, G., FOX, A., FURSENKO, O., GRABOLLA, T., HAAK, U., KNOLL, D., KURPS, R., LISKER, M., MARSCHMEYER, S., RUCKER, H., SCHMIDT, D., SCHMIDT, J., SCHUBERT, M., TILLACK, B., WIPF, C., WOLANSKY, D., and YAMAMOTO, Y., “Sige hbt technology with ft/fmax of 300ghz/500ghz and 2.0 ps cml gate delay,” in *Electron Devices Meeting (IEDM), 2010 IEEE International*, pp. 30.5.1–30.5.4, Dec 2010.
- [9] HYLITIN, T. M., “The beginnings of solid state radar,” *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 36, pp. 1016–1019, Jul 2000.

- [10] KOLIAS, N. J. and BORKOWSKI, M. T., “The development of t/r modules for radar applications,” in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, pp. 1–3, June 2012.
- [11] LAM, K., DING, H., LIU, X., ORNER, B., RASCOE, J., DEWITT, B., MINA, E., and GAUCHER, B., “Wideband millimeter wave pin diode spdt switch using ibm 0.13 um sige technology,” in *Microwave Integrated Circuit Conference, 2007. EuMIC 2007. European*, pp. 108–111, Oct 2007.
- [12] LEUTHER, A., TESSMANN, A., KALLFASS, I., LOSCH, R., SEELMANN-EGGEBERT, M., WADEFALK, N., SCHAFER, F., GALLEGRO PUYOL, J., SCHLECHTWEG, M., MIKULLA, M., and AMBACHER, O., “Metamorphic hemt technology for low-noise applications,” in *Indium Phosphide Related Materials, 2009. IPRM '09. IEEE International Conference on*, pp. 188–191, May 2009.
- [13] MAY, J. and REBEIZ, G., “Design and characterization of w -band sige rfics for passive millimeter-wave imaging,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, pp. 1420–1430, May 2010.
- [14] MEI, X., LIN, C., LEE, L. J., KIM, Y. M., LIU, P. H., LANGE, M., CAVUS, A., TO, R., NISHIMOTO, M., and LAI, R., “A w-band ingaas/inalas/inp hemt low-noise amplifier mmic with 2.5db noise figure and 19.4 db gain at 94ghz,” in *Indium Phosphide and Related Materials, 2008. IPRM 2008. 20th International Conference on*, pp. 1–3, May 2008.
- [15] NASA/JPL, “Cloudsat satellite above earth.” <http://photojournal.jpl.nasa.gov/catalog/PIA03012>, Oct 2005. Artist’s concept of NASA’s CloudSat spacecraft, which will provide the first global survey of cloud properties to better understand their effects on both weather and climate.
- [16] ORNER, B., DAHLSTROM, M., POTHIAWALA, A., RASSEL, R. M., LIU, Q., DING, H., KHATER, M., AHLGREN, D., JOSEPH, A., and DUNN, J., “A bicos technology featuring a 300/330 ghz (ft/fmax) sige hbt for millimeter wave applications,” in *Bipolar/BiCMOS Circuits and Technology Meeting, 2006*, pp. 1–4, Oct 2006.
- [17] ORNER, B., LIU, Q., JOHNSON, J., RASSEL, R., LIU, X., SHERIDAN, D., JOSEPH, A., and GAUCHER, B., “p-i-n diodes for monolithic millimeter wave bicos applications,” in *SiGe Technology and Device Meeting, 2006. ISTDM 2006. Third International*, pp. 1–2, May 2006.
- [18] PAASSCHENS, J. and DE KORT, R., “Modelling the excess noise due to avalanche multiplication in (hetero-junction) bipolar transistors,” in *Bipolar/BiCMOS Circuits and Technology, 2004. Proceedings of the 2004 Meeting*, pp. 108–111, Sept 2004.

- [19] PALMER, HARLAN B., “The capacitance of a parallel-plate capacitor by the schwartz-christoffel transformation,” *American Institute of Electrical Engineers, Transactions of the*, vol. 56, pp. 363–366, March 1937.
- [20] RACETTE, P., HEYMSFIELD, G., LIHUA, L., COOLEY, M., RICHARD, P., and STENGER, P., “A novel dual-band reflector/reflect array antenna: An enabling technology for nasa’s ace radar,” in *Earth Science Technology Forum*, pp. 1–6, 2011.
- [21] RICKELT, M., REIN, H.-M., and ROSE, E., “Influence of impact-ionization-induced instabilities on the maximum usable output voltage of si-bipolar transistors,” *Electron Devices, IEEE Transactions on*, vol. 48, pp. 774–783, Apr 2001.
- [22] SCHMID, R., ULUSOY, A., SONG, P., and CRESSLER, J., “A 94 ghz, 1.4 db insertion loss single-pole double-throw switch using reverse-saturated sige hbts,” *Microwave and Wireless Components Letters, IEEE*, vol. 24, pp. 56–58, Jan 2014.
- [23] SGT. ROBERT S. THOMPSON, “Cobra dane radar.” <http://en.wikipedia.org/wiki/File:Cobradane.jpg>, Jun Date Shot: 1 Jun 1977; Released to Public: 2005. A view of COBRA DANE, an intelligence-gathering phased array radar system specially constructed to monitor Soviet ballistic missile testing on Siberia’s Kamchatka Peninsula. Location: Shemya Air Force Base, Alaska (AK) United States of America (USA).
- [24] SKOLNIK, M., *Radar Handbook, Third Edition*. McGraw-Hill Professional, 2008.
- [25] SOLAR AND SPACE PHYSICS SURVEY COMMITTEE, COMMITTEE ON SOLAR AND SPACE PHYSICS, NATIONAL RESEARCH COUNCIL, *The Sun to the Earth – and Beyond: Panel Reports*. The National Academies Press, 2003.
- [26] STEINHAGEN, F., MASSLER, H., HAYDL, W., HULSMANN, A., and KOHLER, K., “Coplanar w-band spdt and sptt resonated pin diode switches,” in *Microwave Conference, 1999. 29th European*, vol. 2, pp. 53–56, Oct 1999.
- [27] TANELLI, S. AND DURDEN, S.L., IM, E., HEYMSFIELD, G.M., RACETTE, P., and STARR, D.O., “Next-generation spaceborne cloud profiling radars,” in *Radar Conference, 2009 IEEE*, pp. 1–4, May 2009.
- [28] TSAI, Z.-M., YEH, M.-C., LEI, M.-F., CHANG, H.-Y., LIN, C.-S., and WANG, H., “Dc-to-135 ghz and 15-to-135 ghz spdt traveling wave switches using fet-integrated cpw line structure,” in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, pp. 1393–1396, June 2005.
- [29] ULUSOY, A., KAYNAK, M., VALENTA, V., TILLACK, B., and SCHUMACHER, H., “A 110 ghz lna with 20db gain and 4db noise figure in an 0.13 um sige bimos technology,” in *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, pp. 1–3, June 2013.

- [30] UNITED STATES GOVERNMENT - MILITARY, “An/mpq-53 radar for patriot.” http://en.wikipedia.org/wiki/File:Patriot53_.jpg, Jan 2005. The AN/MPQ-53 radar system used by the Patriot for target detection, tracking and missile guidance.
- [31] U.S. ARMY CORPS OF ENGINEERS, “Pave paws radar.” <http://en.wikipedia.org/wiki/File:PAVE.jpg>, March 2006.
- [32] WILLIAMS, D., CORSON, P., SHARMA, J., KRISHNASWAMY, H., TAI, W., GEORGE, Z., RICKETTS, D., WATSON, P., DACQUAY, E., and VOINIGESCU, S., “Calibration-kit design for millimeter-wave silicon integrated circuits,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, pp. 2685–2694, July 2013.
- [33] YANG, Y., CACINA, S., and REBEIZ, G., “A sige bicmos w-band lna with 5.1 db nf at 90 ghz,” in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2013 IEEE*, pp. 1–4, Oct 2013.